



Embedded Capacitor Material

Design and Processing Guidelines for
Printed Circuit Board Fabricators

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Overview

3M™ Embedded Capacitor Material is a planar capacitor material which can be embedded into flexible or rigid printed circuit boards. The material's low impedance allows it to supply charge very rapidly, which is critical for high-speed equipment utilized in the telecommunications, computer, test and measurement, and medical industries. The material's low impedance and high capacitance density enables it to perform the power supply decoupling function so many discrete capacitors can be removed from the board surface. This is especially important in space-constrained applications, such as hand-held electronics and military applications.

This ultra-thin material performs the power supply decoupling much better than discrete components at high frequency. This reduces power bus noise, which can affect signal integrity and cause electromagnetic compatibility (EMC) issues.

3M embedded capacitor material provides high-speed board designers with a superior method of power supply decoupling, so that designs can be operated at the highest frequencies desired. Additionally, the material is compatible with standard printed circuit board processing. This PCB fabricator Design and Processing Guide will inform the board fabricator where deviations from standard circuit board processing are recommended, in order to achieve the best results.

Material Handling

Material handling is the area where the most changes from standard processing will occur. 3M embedded capacitor material has a thin (16 μm), non-reinforced dielectric layer, which is clad with one-ounce (35 μm) copper on each side. The material is flexible and derives most of its stiffness from the copper foil. Having processing equipment with thin core capability is vital, as is operator training in thin core handling. Some fabricators with thin core processing equipment will be able to handle the material with minimal changes from their standard processing; other fabricators will prefer to use leader boards or panel carriers to assist in pre-lamination material transport. A sequential lamination, or "double lamination", process (see below) will also reduce material handling issues. Once the material is laminated into a board or sub-assembly, standard material handling procedures can be utilized.

Process Compatibility

This material is compatible with all standard flex and rigid PCB processing. This includes such things as process sequence, process chemistries and conditions (times, temperatures, concentrations, etc.). Any known exceptions to this will be noted in the following detailed process step information.

Standard vs. Sequential Lamination Process

A sequential lamination process (pattern one side, laminate to a support layer, pattern second side) is recommended to minimize material handling issues. Sequential lamination also offers the benefits of eliminating any design restrictions or having exposed copper at the routed board edges.

Sequential lamination will result in scaling factors that are different for each side of the material. The recommended phototool design guidelines for both sequential and standard lamination processes are described in the following sections.

A. Phototool Design – Sequential Lamination

When a sequential lamination process is utilized, there are no design restrictions. However, it is always a good idea to leave as much copper as possible remaining on the panel for mechanical strength. Copper should only be removed where it is necessary, such as for clearance holes, through-holes, tooling holes, etc. If dam and venting is used for lamination, keep the slot width as small as possible and the slots as far apart as possible.

B. Phototool Design – Standard Lamination

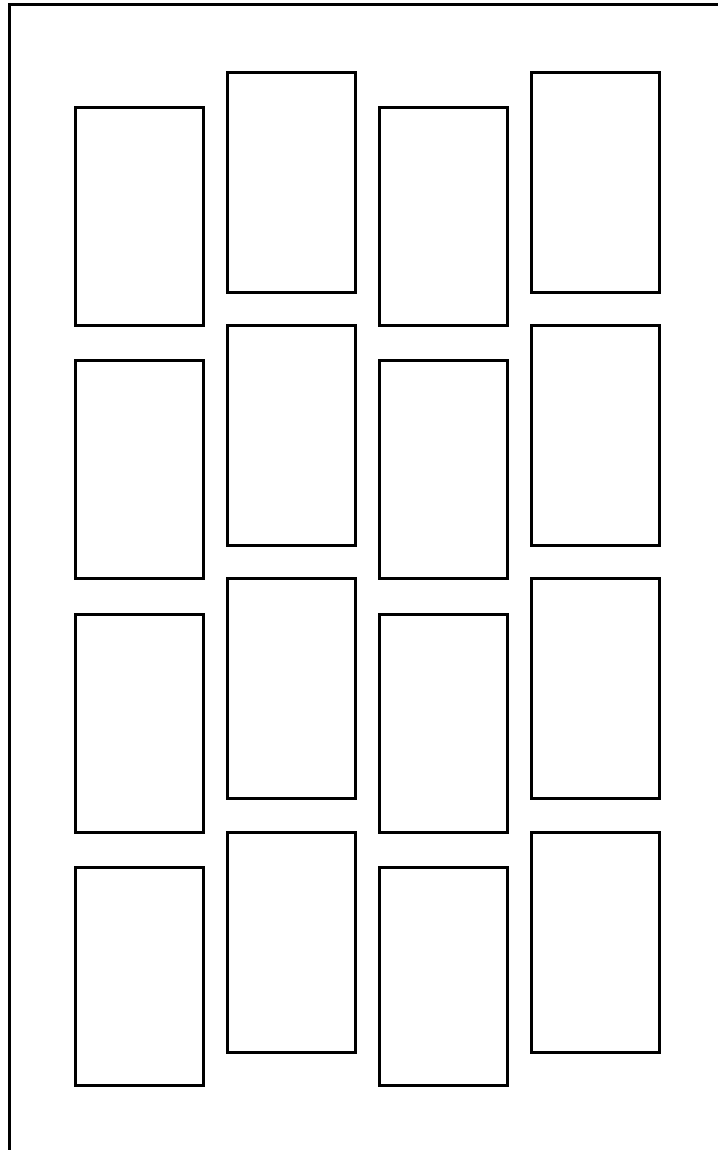
Because this dielectric material is thin and not self-supporting, there are certain design restrictions to make it compatible with standard laminating processes. Below are the guidelines for using 3M™ Embedded Capacitor Material as a distributed capacitor layer (power-ground core) in printed circuits when both sides of the copper are patterned at the same time.

1. One of the copper layers (typically the ground) will need to be extended to the panel edges. This will leave exposed copper at the board edges following routing. It is recommended that the copper at the board edges be electrically isolated from the active board area by using a small copper cut-out, or space, surrounding the active board area (see drawing 1).

2. Leave as much copper on the panel as possible for mechanical strength. Copper should only be removed where it is necessary, such as for clearance holes, through-holes, tooling holes, etc. If venting is used for lamination, keep the slot width as small as possible and the slots as far apart as possible.
3. If split power and/or ground planes are used, the isolation spacing should be kept as small as possible for mechanical strength. However, avoid the use of long, narrow, straight copper cut outs since they can increase the potential for creasing. Additionally, if the panel has a large number up of small boards, each column can be slightly offset from the adjacent columns to increase the rigidity of the panel (see drawing 2).
4. Large areas of copper (one dimension $>0.250''$) must not be removed from opposing sides of the panel in the same location. This will minimize the potential for mechanical damage during material handling and processing.
5. When large-sized areas of copper (one dimension $> 0.250''$) must be removed from opposing sides of the panel in the same general area, a minimum of $0.500''$ (edge-to-edge) should be left between them.



Drawing 1.



Drawing 2.

Board Stack-Up Design

The embedded capacitor layer can be placed anywhere in the board stack-up, including outer layers, if desired. Multiple layers can be used to increase capacitance and lower inductance. Layers can be adjacent to each other, if desired. Placing the embedded capacitor layer closer to the surface (closer to the ICs) will reduce via inductance and make the capacitor material more effective, especially at high frequencies. If more than one embedded capacitor layer is used, the layers should be distributed so there is a balanced stack-up, and board warpage is kept to a minimum.

Inner Layer Processing

The handling of 3M™ Embedded Capacitor Material is comparable to bare two-ounce copper foil. In fact, bare two-ounce foil can be used as a good test vehicle for ensuring the fabricator's inner layer processing capability.

Standard processing speeds, materials and chemistry can be used for wet chemical clean, dry film lamination, UV expose and Develop, Etch and Strip (DES). The material does not have metal tie layers or other adhesion promoters that require special processing. Either acid or ammoniacal cupric chloride etchants can be used. If a standard lamination process is utilized, one slight change is that resist must be brought out to the panel edges on at least one side of the panel ("no postage stamping"). There is also potential for dielectric "blow-out" on very thin dielectric where copper has been removed on both sides in the same area. If a sequential lamination process is used, "postage stamping" can be used on both sides and dielectric "blow out" is not possible.

When conveyerized processing equipment is used, it is critical that enough support rollers are used to properly support the material. If the material is not well supported, the potential exists for denting, creasing and bent corners. If a sequential lamination process is used, it is recommended that the patterned side be face up during the DES process.

Top lighting is recommended at Post-Etch-Punch (PEP). The dielectric and copper have a high contrast that facilitates fiducial recognition. However, the lighting level may need to be modified for best results. It is important to have the material well supported for PEP so the punch makes a clean cut and does not bend the material.

The material is compatible with standard black oxide, reduced oxide or alternative oxide processes. Some fabricators prefer thin core horizontal alternative oxide processes to the typical vertical (dip tanks) oxide process because they provide improved material handling. The 3M™ Embedded Capacitor Material utilizes a rolled (RA) copper, which is inherently smoother than most electrodeposited (ED) copper foil. Some fabricators have found it useful to increase the amount of microetch in the oxide or alternative oxide process to better roughen the copper surface so that it more resembles an ED surface roughness.

Inner Layer Inspection and Test

Standard settings for Automated Optical Inspection (AOI) can be used. Because the copper and dielectric have high contrast, the level of lighting may have to be adjusted. 3M embedded capacitor material can be electrically tested (HiPot) for insulation resistance similar to other cores. However, the material will charge for a very short duration of the test. Measurement of the insulation resistance must not occur until after the capacitor material has charged, otherwise the tester could sense the charging current as a leakage current and indicate a failure. The panel should be discharged prior to being removed from the tester. Since the dielectric material is

much thinner than standard core material, the HiPot should be set at the voltage specified by 3M for the dielectric thickness of the material.

If desired, capacitance and dissipation factor (loss tangent) can be directly measured with some modifications to the tester. This can also be done at final e-test. In the case of sequential lamination, the panels must be measured after the first patterning process because there is no electrical access to the first-patterned side after lamination.

Lay-Up and Lamination

Care must be used in the lay-up of 3M™ Embedded Capacitor Material, especially when a non-sequential lamination process is utilized. It is possible to stretch the flexible material over the fixture pins if proper procedures are not followed. Fabricators who utilize bare copper foil in lay-ups should follow the same material handling procedures for the lay-up of embedded capacitor material as they do for bare copper foil.

For sequential lamination sub-parts, there are no significant material handling issues. For sequential lamination, cleanliness at lay-up is paramount. If epoxy dust or chips are present, they can be transferred to the copper surface. This can result in unetched copper in clearance holes, which can cause shorting on final product. Standard FR-4 lamination times, temperatures and pressures can be used. However, the maximum recommended lamination temperature is approximately 200°C (400°F). Multiple and lengthy (several hours) lamination cure cycles are not an issue as long as the maximum temperature is not exceeded.

Scaling factors for non-reinforced embedded capacitor material may be different than for FR-4. If a sequential lamination process is used, each side will likely have a different scaling factor. 3M embedded capacitor material scaling factors will be dependent on the lamination process parameters and adjacent materials in the stack-up. Different designs will likely have different scaling factors. However, once the scaling factors have been determined for a particular design, the scaling factors will be accurate for subsequent lots (as long as press parameters are not changed). An initial ballpark scaling factor for the first etched side in a sequential lamination process would be to use the same scaling factor as the material it will be laminated to. Since the second side will have gone through a lamination process prior to imaging, the scaling factors for the second side should be significantly less than for that used for the first side patterned.

Drill, Deburr and Through-Hole Processing

Standard FR-4 drill (speeds, feeds, etc.) and post-drill deburr process parameters can be used. The embedded capacitor material is thin and contains extremely small ceramic (BaTiO_3) particles, no effect on drill life has been seen or is anticipated. The material is compatible with all standard wet chemical desmear/etchback chemistries and metallization chemistries. No changes in the FR-4 desmear/metallization process are required.

A plasma desmear process (alone or in combination with wet chemical) can be used with the embedded capacitor material. It is highly recommended that a bake be utilized prior to plasma (or as part of the plasma process) to remove moisture. Additionally, only a desmear (no significant etchback) should be used unless the plasma process is used in combination with a wet chemical desmear process. Finally, when only a plasma desmear is utilized, a wet chemical through-hole cleaning is required prior to subsequent metallization.

Microvia Processing

The material is fully compatible with microvia processes including laser drilling. The material can be easily laser drilled (UV-YAG; 355 or 266 nm). The material is compatible with standard post-laser drilling cleaning and metallization processes.

Outer Layer Processing

This material is compatible with all outer layer processing, including imaging, plating and strip and etch. No changes in standard processing are required.

Solder Mask, Surface Finish and Rout

3M™ Embedded Capacitor Material is compatible with all standard solder mask processing. The solder mask thermal cure temperature should not exceed 200° C (392° F). The material is also compatible with all common surface finishes, including organic solderability preservatives (OSP), hot air solder leveling (HASL), immersion silver and electroless nickel-immersion gold (ENIG). No changes to standard solder mask or surface finishing are required. 3M recommends extending the bake cycle time by at least 50 percent, prior to HASL, to ensure all moisture is removed.

No changes are required for the routing process. However, it should be noted that if a non-sequential lamination process was used, routing through copper on one side of the material will be required.

Final Inspection and Electrical Test

No changes in final inspection or electrical test are required with the exception of ensuring that charging of the capacitor material is not indicating a false leakage current. This testing should be conducted at the voltage specified by 3M for the dielectric thickness of the material. The PCB process does not have any significant impact on the capacitance or dissipation factor of the material. Thus, if the material meets the criteria when tested at inner layer, it should still meet the

criteria at final electrical test. If desired, the capacitance and dissipation factor (loss tangent) can be measured with an LCR meter or other appropriate test equipment.

Summary

3M™ Embedded Capacitor Material is compatible with all standard FR-4 processing, including laser drilling. Some slight process modifications, mostly related to material handling, will be necessary to successfully work with the material. The material handling issues can be minimized by proper design, utilizing a sequential lamination process, and optimized handling procedures. A sequential lamination process is strongly recommended to ease material handling, eliminate design restrictions and prevent unsupported dielectric damage.

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