Using Embedded Capacitance to Improve Electrical Performance, Eliminate Capacitors and Reduce Board Size in High Speed Digital and RF Applications

Joel S. Peiffer
3M Company
3M Center, MS: 201-1E-21
St. Paul, MN 55144
651-575-1464; 651-736-2947 (fax)
jspeiffer@mmm.com

Background

The global electronics industry is exhibiting a widespread and growing interest in the technology of embedded passives. This interest can be attributed to three primary benefits. First, embedded passives have far less parasitic inductance than discrete components, which enables electrical performance advantages in high speed digital applications. Second, embedding saves surface real estate, which allows for board size reductions. Third, the incremental cost of embedding additional passive components is typically negligible, which suggests the potential for system cost reduction in designs with high passive component counts.

3M™ Embedded Capacitor Material is a high performance embedded passive material intended for embedded capacitor applications. It is a copper-clad laminate which utilizes an ultra-thin, high K-value dielectric material between the copper planes to deliver a capacitance density of over 6 nF/in^2.

This presentation will focus on this laminate material and how it can be used to improve electrical performance and reduce board size (by replacing discrete capacitors), and will also address the impact on PCB reliability and system cost.

Electrical Performance Advantages

Moore's law continues to drive the semiconductor industry, shrinking feature sizes and sending transistor counts higher. Along with these changes comes lower operating voltages and increased current requirements. According to the Semiconductor Industry Association and NEMI roadmaps (Table 1), current, voltage and power trends will continue for the foreseeable future.

Table 1

SIA Roadmap	**'01**	**'02**	**'03**	**'04**	**'05**	**'06**	**'07**	**'10**	**'13**	**'16**
Power Supply Voltage (V) Vdd (High Performance)	1.1	1.0	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Allowable Max Power (W) High Performance with Heatsink	130	140	150	160	170	180	190	218	251	288
NEMI Roadmap	**'01**	**'02**	**'03**	**'04**	**'05**	**'06**	**'07**	**'10**	**'13**	**'16**
Max Power/Device (W) Large Business Machine Products			200		225		225	240	280	300
Max Current/Device (A) Large Business Machine Products			200		250		280	300	350	375

These trends place severe demands on the ability of the circuit board to distribute power to the surface-mounted active devices. The circuit board's power distribution system must meet increasingly low impedance requirements.

The typical components of a circuit board's power distribution system include a switching power supply, bulk decoupling capacitors, high frequency decoupling capacitors and inner layer power and ground planes. One of the best ways to improve power distribution (i.e. decrease impedance) is to use closely spaced power and ground planes within the multilayer board stack up. This approach has been used for over 20 years with FR-4 dielectrics in the range of 2 to 4 mils in thickness.

The use of thinner, high dielectric constant (k) dielectrics can significantly increase the effectiveness of this approach. Standard FR-4 technology is limited to 2 mils thickness, a k value of approximately 4 and a capacitance density of only 0.5 nF/in^2. Thinner (<25 um) dielectric materials, especially those filled with high dielectric ceramic particles, are now being used to address the power distribution issues of today's high frequency designs.

One such material is 3M's embedded capacitor material, offered in a range of dielectric thicknesses from 8 to 14 microns (0.31 to 0.55 mils) and a k of 16. In combination, these features deliver a high capacitance density of 6.4 nF/in^2 to ~10.5 nF/in^2 and offer many benefits when used for decoupling high speed digital electronics, including:

- Lowers impedance of power distribution system
- Dampens board resonances
- Reduces noise on power plane
- Reduces radiated emissions
- Can replace large numbers of discrete decoupling capacitors

From a designer's perspective, noise margins are increased, which can translate into improved performance and less engineering time devoted to troubleshooting and fixing noise problems. In addition, the component count reduction saves time in board layout.

Examples of Electrical Performance Improvement in High Speed Digital Board Designs
Below are several examples of high speed digital board designs that used ultra-thin dielectric with a dielectric constant (k) of 16 for distributed decoupling (power-ground) in multilayer rigid printed circuit boards.

In the first example (Figure 1), the self-impedance of a 5" X 10" multilayer bare board with ultra-thin (8 um) dielectric between the power and ground planes is compared to the same board design with 50 um (2 mil) thick FR-4 and 25 um (1 mil) thick FR-4 dielectric between the power and ground planes.

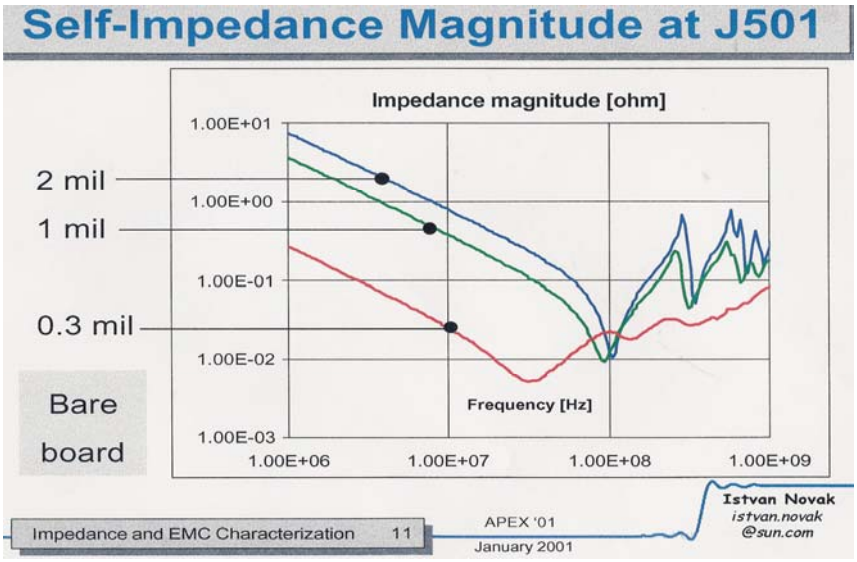

Figure 1 – Self-Impedance vs. Frequency

(Courtesy of Sun Microsystems)

At lower frequencies, it can be seen that the self-impedance of the ultra-thin laminate material is more than an order of magnitude lower than that of 1 or 2 mil thick FR-4. This is due to the much higher capacitance density of the ultra-thin material (~10 nF/in^2 vs. ~0.5 - 1 nF/in^2). At higher frequencies, the self-impedance of the ultra-thin dielectric material is also significantly lower than that of the 1 or 2 mil FR-4 laminate. This is primarily due to the significantly lower self-inductance of the ultra-thin material. Finally, in the 100 MHz to 1 GHz frequency range, both the 1 mil and 2 mil FR-4 laminates show very large impedance spikes caused by board resonances. These are very undesirable as the noise associated with these impedance spikes can trigger false switching, signal integrity and EMI issues. However, in the case of the ultra-thin dielectric, the board resonances are almost completely damped due to the high copper losses of closely spaced power and ground planes at high frequencies.

In figure 2, the self-impedance of ultra-thin embedded capacitor laminates with dielectric thickness of 8 um, 12 um and 24 um all with a k of 16 are compared to a 50 um FR-4 laminate with a k of ~4 on this same board design. Here it can be seen that the 24 um material with a k of 16 performs much better than a 25 um laminate with a k of 4 (shown in Figure 1). Additionally, the 12 um material performed nearly as well as the 8 um material in both providing a low impedance in the pre-resonance frequency as well as dampening the noise due to board resonances at higher frequencies.

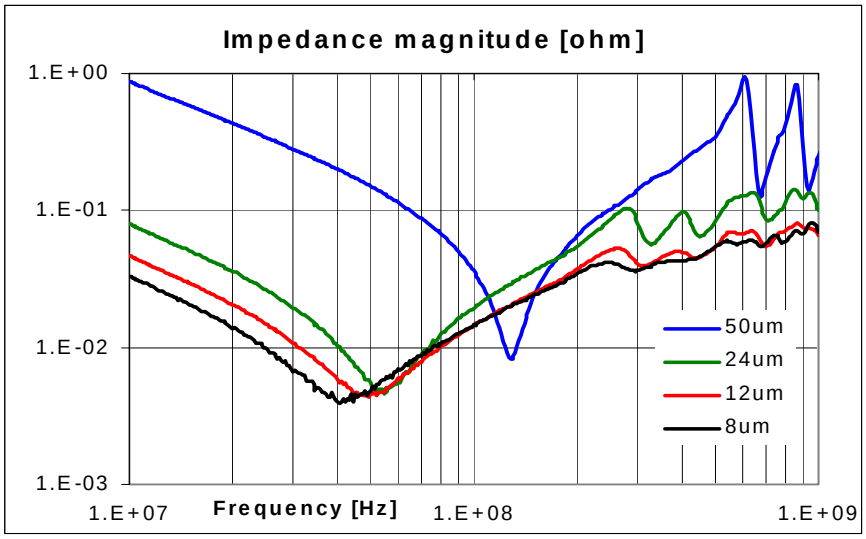

Figure 2 – Impedance vs. Frequency
(Courtesy of Sun Microsystems)

In figure 3, the close-field radiation was measured on the same 5" X 10" board as above. The measurement was taken on the long (10") side of the board, approximately one-half inch from the edge of the board. Here it can be seen that the ultra-thin dielectric is responsible for lowering the EMI (noise seen on all samples at >200 MHz is due to cable effects and should be ignored).

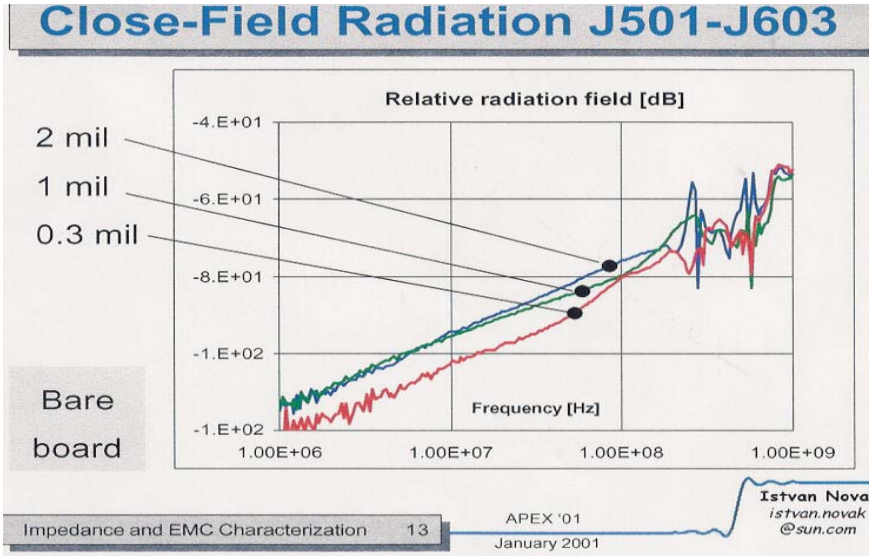

Figure 3 – EMI vs. Frequency
(Courtesy of Sun Microsystems)

In another example, the S21 or transfer function of noise from one part of a board to another was measured (a lower S21 is better). The board size was 10" X 12" (see Figure 4). A "typical" four metal layer board with 35 mil separation between power (layer 2) and ground (layer 3) was compared to a board with a 16 um thick (k of 16) dielectric layer between power and ground. The typical board had 99, 0.1 uF SMT decoupling capacitors assembled uniformly over the board surface. The ultra-thin embedded capacitance board had no decoupling capacitors mounted.

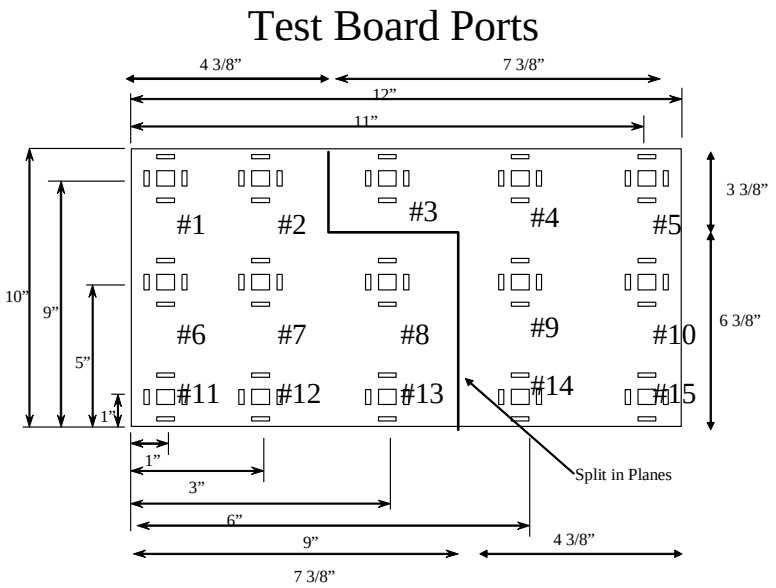

Figure 4
(Courtesy of IBM)

As can be seen in Figure 5, the typical board, even with a large amount of discrete decoupling capacitance (9900 nF), was only able to achieve low S21 at below several hundred MHz. Whereas, the board with ultra-thin embedded capacitance (Figure 5) had an extremely low S21 over the entire frequency range (up to 15 GHz). In the frequency range over 500 MHz,, the ultra-thin embedded capacitance board had a S21 of about 40 dB less than that of the typical board.

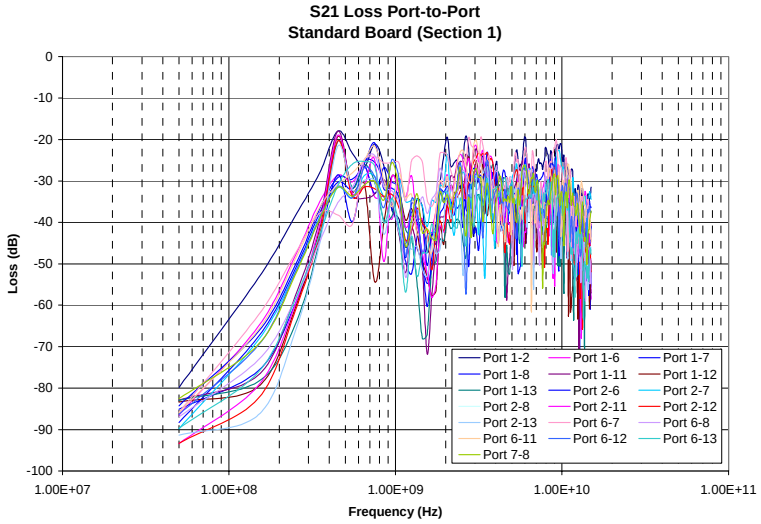

Figure 5 – S21 of Typical Board
(Courtesy of IBM)

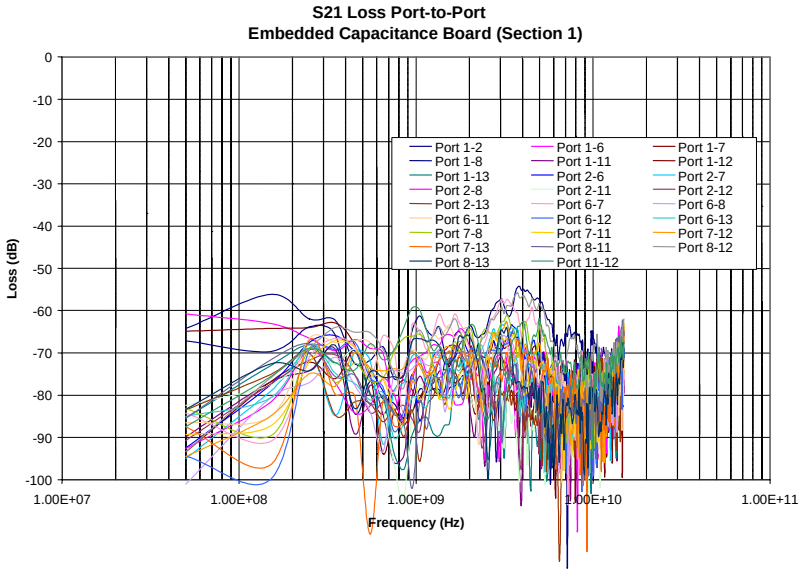

Figure 6 – S21 for Embedded Capacitance Board
(Courtesy of IBM)

In figure 7, the noise versus frequency was measured on a fully assembled daughter board with an approximate size of 5" X 5". The noise was measured on the 1.5 volt plane up to a frequency of ~1.5 GHz. The daughter card had a MIPS R14K processor running at 550 MHz and 9 secondary cache SRAMs running at 275 MHz.

Two board designs were compared. The first had a 3 mil FR-4 dielectric thickness between power and ground planes and the second board had an 8 um dielectric thickness (with a k of 16) between power and ground planes.

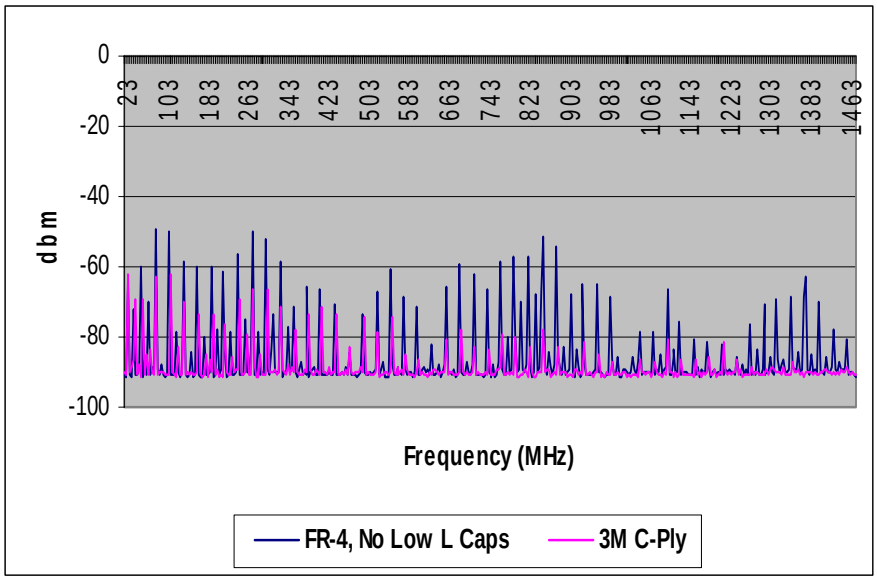

Figure 7 – Power Bus Noise vs. Frequency
(Courtesy of H.P.)

As can be seen in Figure 7 above, the board with the ultra-thin dielectric had significantly less noise at all frequencies above ~50 MHz. At frequencies above 500 MHz, the board with the 3 mil FR-4 still had had a large amount of noise whereas the board with the ultra-thin dielectric had extremely effective noise dampening above 500 MHz. Over the frequency range measured, the board with the 8 um dielectric (k of 16) had 13.3 dB less noise than that of the board with the 3 mil FR-4 power ground plane.

The peak-to-peak voltage ripple was also measured on these boards. For the case of the board with the 3 mil FR-4 power-ground plane spacing, the peak-to-peak noise was 235 mV(15.7% of 1.5V). For the board with the 8 um power-ground spacing, the voltage ripple was 114 mV (7.6% of 1.5V), or slightly less than one-half of that of the 3 mil FR-4 board.

As part of the National Center for Manufacturing and Sciences (NCMS) Embedded Decoupling Capacitance (EDC) industry consortia, power bus noise and voltage fluctuation were measured by the University of Missouri at Rolla. The six metal layer boards were 2" X 3" in size. Each contained a 50 MHz oscillator, a 22 uF bulk decoupling capacitor, eight octal clock drivers and a number of load capacitors.

The materials used for layers 3 (power) and 4 (ground) of the boards were various embedded capacitance laminate materials including 2 mil FR-4 (BC2000^{TM}) and the 3M^{TM} Embedded Capacitor Material (5 um; k of 16). These boards were compared to a baseline board with an approximate 4 mil FR-4 laminate used for the power-ground core.

None of the boards with embedded capacitance laminates were surface mounted with any decoupling capacitors beyond the 22 uF bulk decoupling capacitor. The baseline board was surface mounted with 33, 0.01 uF high frequency decoupling capacitors (total of 330 nF). The amount of embedded capacitance for the 2 mil embedded capacitance board was ~3 nF and was ~107 nF for the 5 um embedded capacitance laminate board.

First, the 5 um laminate board (with no decoupling capacitors) was compared to the 4 mil FR-4 baseline board, with and without the 33, .01 uF decoupling capacitors over the frequency range of 1 MHz to 5 GHz (Figure 8). Here it can be seen that the .01 uF decoupling caps did a reasonably good job decoupling in the 1 MHz to 1 GHz range on average. However, at frequencies beyond 1 GHz, the decoupling capacitors are completely ineffective due to their high inductance. The 5 um laminate did a much better job of decoupling across the entire frequency range (10 to 40 dB noise reduction) even though it had only one-third of the capacitance (107 nF vs. 330 nF) of the SMT decoupling capacitors.

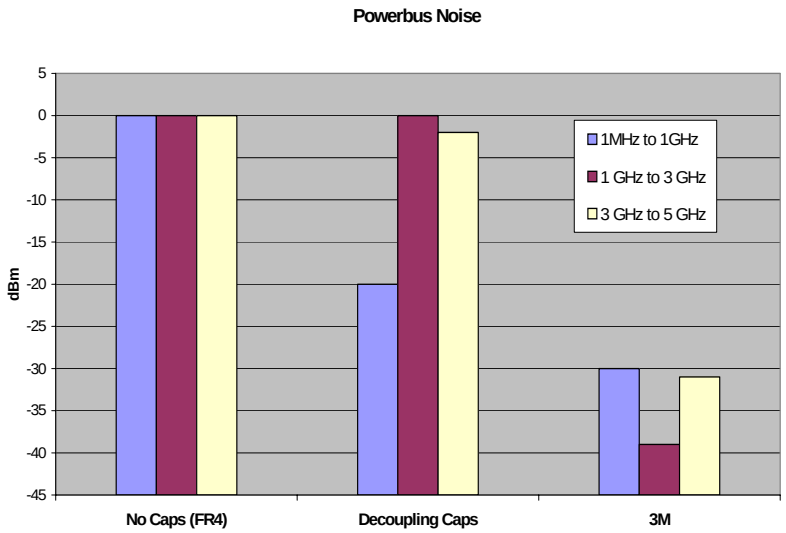

Figure 8 – Power Bus Noise
(Courtesy of University of Missouri at Rolla)

Power bus voltage ripple measurements were also taken on the embedded capacitor and baseline 6 metal layer boards (Figure 9). Below the amount of voltage fluctuation from the nominal 3.3 volt power plane are shown in the time domain for the 4 mil FR-4 baseline board with 33 decoupling capacitors, the 2 mil FR-4 board and the 5 um board.

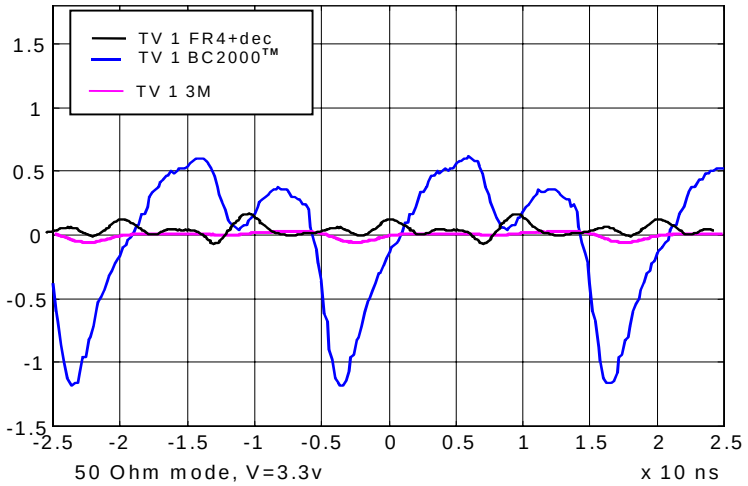

Figure 9 – Power Plane Voltage Fluctuation

(Courtesy of University of Missouri at Rolla)

The peak-to-peak voltage ripple for these three boards is shown below in Table 2. Here it can be seen that the board with the 5 um embedded capacitance material had less than one-half the voltage ripple even though it had less than one-third of the capacitance of the SMT caps. The board with the 2 mil FR-4 embedded capacitance had such a large voltage fluctuation that it did not function properly. This was due to the lack of sufficient embedded capacitance to provide charge to the IC until the bulk decoupling capacitor could provide charge.

Table 2 – Peak-to-Peak Noise Measurements
(Courtesy of University of Missouri at Rolla)

Type of Board	Capacitance (nF)	Vpp (mV)
4 mil FR-4 with SMT decoupling	330	214
BC2000 (50 um)	3	1,740
3M (5 um)	107	89

Board Size Reduction and Capacitor Elimination in High Speed Digital Board Designs
3M's embedded capacitor laminate material has been successfully implemented on a number of OEM designs to replace large quantities of discrete decoupling capacitors from the board surface. Some of the data from these board designs is shown in Table 3. Here it can be seen that in every case, the use of the distributed embedded capacitance allowed the elimination of at least 60% of the discrete capacitors. In most cases it was at least 75% and in two cases, all of the discrete decoupling capacitors were removed. In one case, over 500 capacitors were eliminated from the board design. It is also very important to note that only a very small amount of embedded capacitance was needed to replace a very large amount of discrete capacitance (each nF of embedded capacitance replaced 10 to 40 nF of discrete capacitance).

Table 3

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	Ratio of Removed to Embedded	% of Total Discrete Caps Removed
EDC TV1	**330** *33 x 0.01 uF*	**105**	**3.1**	**100%**
OEM A	**12,600** *126 x 0.1 uF*	**300**	**42.0**	**>75%**
OEM B	**6,310** *62 x 0.1 uF* *11 x 0.01 uF*	**210**	**30.0**	**>60%**
OEM C	**3,180** *29 x 0.1 uF* *28 x 0.01 uF*	**305**	**10.4**	**>75%**
OEM D	**52,900** *529 x 0.1 uF*	**1970**	**26.9**	**>75%**
OEM E TV	**9,900** *99 X 0.1 uF*	**660**	**15.0**	**100%**
OEM F	**~35,000** *443 total (mostly 0.1 uF)*	**~1000**	**~35**	**100%**

Table 4 provides additional information including the board size and number of embedded capacitor laminate cores used in each of these test cases. From this it can be seen that this ultra-thin embedded capacitor material has proven capable of removing 3 to 6 capacitors per square inch of board surface area with only one or two cores in the board stack up. On larger sized boards, this can allow the elimination of well over 500 capacitors.

Table 4

Design	Board Layers	No. of 3M ECM Power-Ground Cores	Approx. Board Area (in^2)	Total No. of Caps Removed	Caps Removed per sq in
EDC TV1	**6**	**1**	**6**	**33**	**5.5***
OEM A	**12**	**1**	**35**	**126**	**3.6**
OEM B	**10**	**2**	**17**	**73**	**4.3**
OEM C	**8**	**2**	**12**	**57**	**4.6**
OEM D	**14**	**2**	**121**	**529**	**4.4**
OEM E TV	**4**	**1**	**120**	**99**	**0.8***
OEM F	**14**	**2**	**~100**	**443**	**~4.4***

* indicates that 100% of high frequency decoupling capacitors were removed from board

Finally, Table 5 presents the results of electrical performance testing. This includes functional testing as well as (in some cases) power bus noise and EMI testing. In all cases, the boards were found to be functional. In three cases tested, there was a very significant reduction in power bus noise. In the three cases where EMI was tested, there was no increase in EMI. In fact, in one case, there was some EMI reduction and in another, there was significant reduction.

Table 5

Design	Discrete Cap. Removed (nF)	Functionality Testing	Power Bus Noise	EMI
EDC TV1*	**330** *33 x 0.01 uF*	**Fully Functional**	**Much Improved (90 vs. 230 mV)**	**Somewhat Better**
OEM A	**12,600** *126 x 0.1 uF*	**Fully Functional**	**Not Tested**	**Not Tested**
OEM B	**6,310** *62 x 0.1 uF; 11 x 0.01 uF*	**Fully Functional**	**Not Tested**	**Similar**
OEM C	**3,180** *29 x 0.1 uF; 28 x 0.01 uF*	**Fully Functional (>2 yrs at 24/7)**	**Not Tested**	**Not Tested**
OEM D	**52,900** *529 x 0.1 uF*	**Fully Functional**	**Not Tested**	**Much Better (10-15 dB)**
OEM D TV*	**1,600** *16 X 0.1 uF*	**Fully Functional**	**Much Improved (20 vs. 120 mV)**	**Not Tested**
OEM E TV*	**9,900** *99 X 0.1 uF*	**Fully Functional**	**Much Improved (30 dB+)**	**Not Tested**
OEM F*	**~35,000** *443 total (mostly 0.1 uF)*	**Fully Functional**	**Not Tested**	**Not Tested**

In summary, this data suggests that by utilizing a few hundred nanofarads of low inductance, embedded distributed capacitance (as a power-ground core or cores), a very large number of surface mounted decoupling capacitors can be

removed. It is strongly believed that all decoupling capacitors under 0.1 uF can be removed as well as the majority of 0.1 uF decoupling capacitors. For high speed designs, this can result in the removal of many hundreds of capacitors. This is also very significant for portable and military products where the desire for board area reduction is paramount.

Board Size Reduction and Capacitor Elimination in RF Board Designs

The above data were examples of using embedded distributed (power-ground) capacitance to remove discrete decoupling capacitors in high speed digital designs. The 3M material can also be used in RF applications such as modules for cell phones to remove large numbers of capacitors.

In one such design where there was a significant RF noise issue, the material was used in place of discrete capacitors due to board size constraints. In this application where the embedded capacitor material was used for RF filtering, an extremely high density of capacitors (>50 caps/in^2) were not required due to a combination of the high capacitance density of the material and the low capacitance requirements (<100 pF) of the capacitors.

In this case, the noise problem was very successfully solved (>20 dB reduction) and no board size increase was required due to adding discrete capacitors to the board surface. If the board had used discrete surface mount capacitors, the noise reduction seen may have been less (due to higher inductance) and it would have required a significant increase in board size and/or board layers.

The above program has been extremely successful. The embedded capacitance material was designed, tested, qualified and ramped to high volume production in approximately 9 months. In 2007, it is anticipated that over 80 million cell phones will have been manufactured with the ultra-thin (14 um), high capacitance (6.4 nF/in^2) material. This includes shipments to over 10 cell phone manufacturers around the world including several Tier 1 cell phone manufacturers.

Cost Reduction

The use of ultra-thin power-ground cores for embedded distributed capacitance has potential to lower the system level cost of many products. However, the assessment of potential system level cost reduction is very complex. Ultra-thin embedded capacitor materials currently cost significantly more than standard laminate material. They can also cost significantly more to process due to their material handling requirements. These increased costs may be offset by the ability to get more boards up on a panel or by a reduction in the total number of board layers. It may also be possible to combine two or more boards in a system into the same board. However, in general, unless there is significant board size reduction, bare board costs of embedded capacitor boards will be significantly more than traditional bare boards.

As previously mentioned, the use of ultra-thin power-ground cores can also be used to eliminate large numbers of discrete power supply decoupling capacitors from the board surface. When all of the costs associated with the drilling of the capacitor vias, and the purchase and assembly of the discrete capacitors (assembly, inspection, rework, etc.) are combined, it can represent a very significant cost reduction per board, especially if assembly can be reduced from double to single sided.

There may be additional cost reduction available with the use of ultra-thin embedded capacitor materials. Embedded capacitor materials can reduce or eliminate EMC issues. This may provide cost savings associated with EMI shielding and containment. Additional cost reduction is possible by fewer or shorter design cycles, but this can be difficult to quantify. Removing the discrete capacitors improves board long term reliability because solder joint and via failures are reduced. Bare board yields can improve due to the elimination of vias, board size reduction and increased routing space. On the other hand, material handling or other processing issues with embedded capacitor materials could have a significant negative effect on board yield, if care is not taken in board design and processing as explained in the next section. Another factor is that rework is not possible with embedded capacitor materials once the material has been laminated into a board.

In summary, some inputs into the cost comparison can be easily understood and quantified while many others cannot. Some factors increase the system level cost while others decrease it. There are also a number of inputs that can increase or decrease system level cost depending on the material involved and the design and manufacture of the boards.

There are three important items to remember when considering potential cost reduction with the use of embedded capacitor materials. The first is to always consider total system cost, not bare board or assembled board costs. The second is to compare not only what the system level cost is at the current time but what it will be throughout the life of the product. Thirdly, it should be kept in mind that as the supply chain grows, gains experience, and becomes more competitive, the costs associated with the use of these materials will continue to decrease which will make system cost reductions possible in a greater number and variety of applications.

Compatibility with PCB Fabrication Processes

The 3M copper-clad laminate material is epoxy-based and is compatible with standard flex and rigid PCB materials and processing. This includes processes such as DES, traditional and alternative oxides, plasma or wet chemical desmear, plated-thru-hole metallization, laser drilling, conductive or non-conductive via fills and electrical test. With a few minor exceptions, the fabricators standard FR-4 process is used as is.

Material handling is where most changes from standard processing will occur. The embedded capacitor material has a thin (8-14 µm), non-reinforced dielectric layer, with one-ounce (35 µm) copper on each side. The material is flexible and derives most of its stiffness from the copper foil. Having processing equipment with thin core capability is vital, as is operator training in thin core handling. Some fabricators with thin core processing equipment will be able to handle the material with minimal changes from their standard processing; other fabricators will prefer to use leader boards or panel carriers to assist in pre-lamination material transport. A sequential lamination, or "double lamination", process (see below) will also reduce material handling issues. Once the material is laminated into a board or sub-assembly, standard material handling procedures can be utilized.

A sequential lamination process (pattern one side, laminate to a support layer, pattern second side) is recommended to minimize material handling issues. Sequential lamination also offers the benefits of eliminating any design restrictions or having exposed copper at the routed board edges. Sequential lamination will result in scaling factors that are different for each side of the material.

When a sequential lamination process is utilized, there are no design restrictions. However, it is always a good idea to leave as much copper as possible remaining on the panel for mechanical strength. Copper should only be removed where it is necessary, such as for clearance holes, through-holes, tooling holes, etc. If dam and venting is used for lamination, keep the slot width as small as possible and the slots as far apart as possible.

The embedded capacitor layer can be placed anywhere in the board stack-up although internal layers are usually recommended. Multiple layers can be used to increase capacitance and lower inductance. Layers can be adjacent to each other, if desired. Placing the embedded capacitor layer closer to the surface (closer to the ICs) will reduce via inductance and make the capacitor material more effective, especially at high frequencies. If more than one embedded capacitor layer is used, the layers should be distributed so there is a balanced stack-up, and potential board warpage is kept to a minimum.

In summary, 3M^{TM} Embedded Capacitor Material is compatible with standard PCB processing, including laser drilling (Figure 10). Some slight process modifications, mostly related to material handling, will be necessary to successfully work with the material. The material handling issues can be minimized by proper design, utilizing a sequential lamination process, and optimized handling procedures. A sequential lamination process is strongly recommended to ease material handling, eliminate design restrictions and prevent unsupported dielectric damage. Additional information on design and processing can be found in the 3M^{TM} Embedded Capacitor Material Design and Processing Guidelines for Printed Circuit Board Fabricators which is available on the following web site (http://www.3m.com/us/electronics_mfg/microelectronic_packaging/materials/index.jhtml).

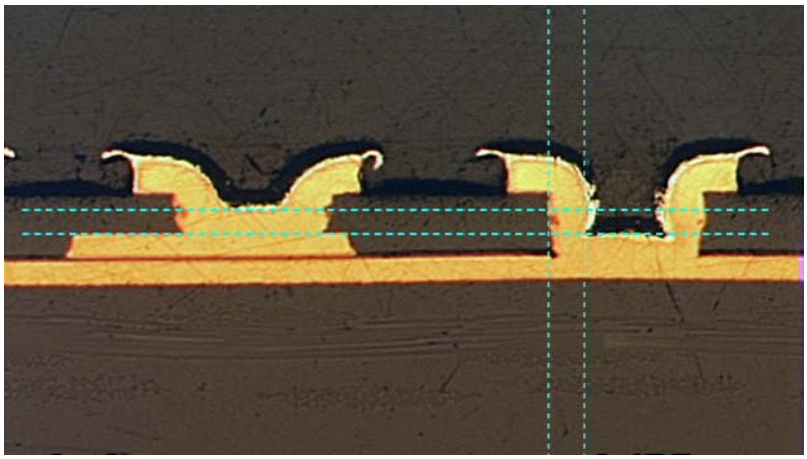

Figure 10 – Microvias in Test Board
(Courtesy of Merix)

Reliability

A large amount of internal and external reliability testing has been completed over the last ten years. This includes numerous designs from a large number of PCB fabricators. The ultra-thin (k of 16) embedded capacitor material has shown to be a reliable material for use in multilayer rigid printed circuit boards. These designs have consisted of anywhere from four to over 40 metal layers with anywhere from one to approximately a dozen embedded capacitor cores.

Since 1996, many hundreds of multilayer boards from over a dozen PCB fabricators have been tested using the following industry reliability tests seen in Table 5 below.

Table 5 – Reliability Tests

Electrostatic Discharge (ESD)
High Potential (HiPot)
Life (high temp exposure with bias)
Mechanical (bend)
Multiple Solder Float
Multiple Solder Reflow (incl. lead free)(Figure 10)
Temperature, Humidity (with and without bias)
Thermal Cycle
Thermal Shock
TMA 260 (time to delamination)
Vibration

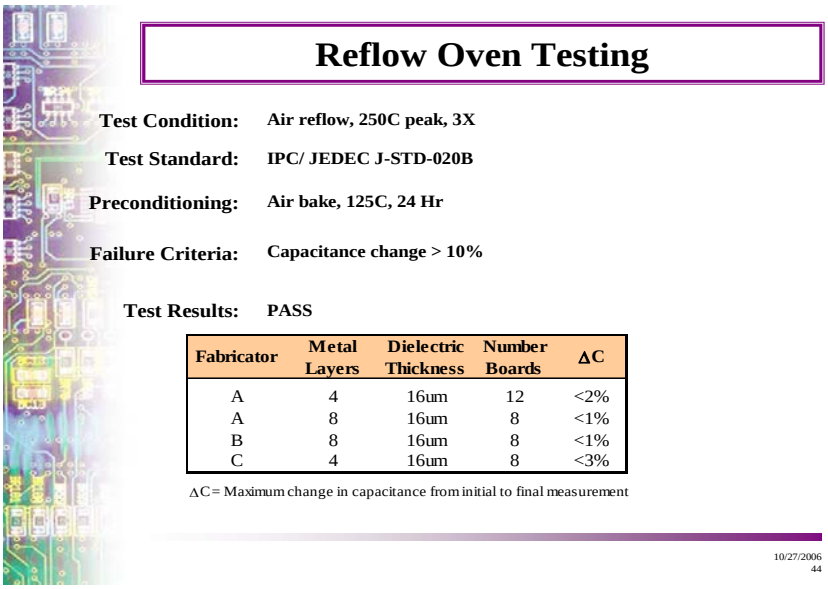

Figure 10 – Lead Free Reflow Simulation

Electrical tests and properties measured included capacitance, dissipation factor, insulation resistance/leakage current, and via resistance. The test results have been very positive. The ultra-thin embedded capacitor material passes all tests with no significant changes to electrical properties or issues with board reliability including plated-through-hole reliability. Visual inspection of boards from multiple fabricators has shown all of them to pass MIL-PRF-31032, even after 6 solder floats at 288C.

The only tests which had an effect on electrical properties were high temperature, high humidity tests. In these tests, both the capacitance and dissipation factor increased due to moisture absorption. After baking, these properties returned to their pre-test levels. The same effect was seen in boards with high Tg FR-4 power-ground cores. Overall, the reliability of the ultra-thin embedded capacitor material has been shown to be very similar to high glass transition temperature FR-4 power-ground cores. In some cases (ESD, TMA 260 and lead free reflow), they outperformed high Tg, FR-4 materials.

Commercialization Status and Market Segment Interest

3M's embedded capacitor material (14 um) has been commercially available since April 2004. The product is RoHS compliant and does not contain bromine. It received UL certification in 2001. Manufacturing is done on a high volume production line at a 3M facility in North America, and lead times (order-to-ship) are typically under 5 days.

Thinner (11 um and 8 um) embedded capacitor laminates which have even higher capacitance densities (up to ~11 nF/in^2) are also being developed. These materials are available as pre-commercial materials for engineering evaluation. Additionally, 3M is developing a resistor-capacitor (R-C) laminate material (Figure 11). In this case, one or both of the bare copper foils is replaced with copper foil having a thin-metal resistive layer. The sheet resistance of the thin-film resistor material is typically in the 10 – 1000 ohms per square. The obvious advantages of combining resistive and capacitive structures into the same substrate include cost reduction, space reduction and electrical performance improvements. However, other potential advantages include improved power ratings of the resistors (due to the close proximity of the additional copper layer), improved ESD resistance of the embedded resistors as well as potential improvement in the embedded capacitance material abilities to dampen noise at high frequency (due to the presence of embedded resistor material adjacent to the dielectric layer where most of the current flow takes place). Initial testing of the R-C laminate material (25 and 1000 ohm per square) has been positive.

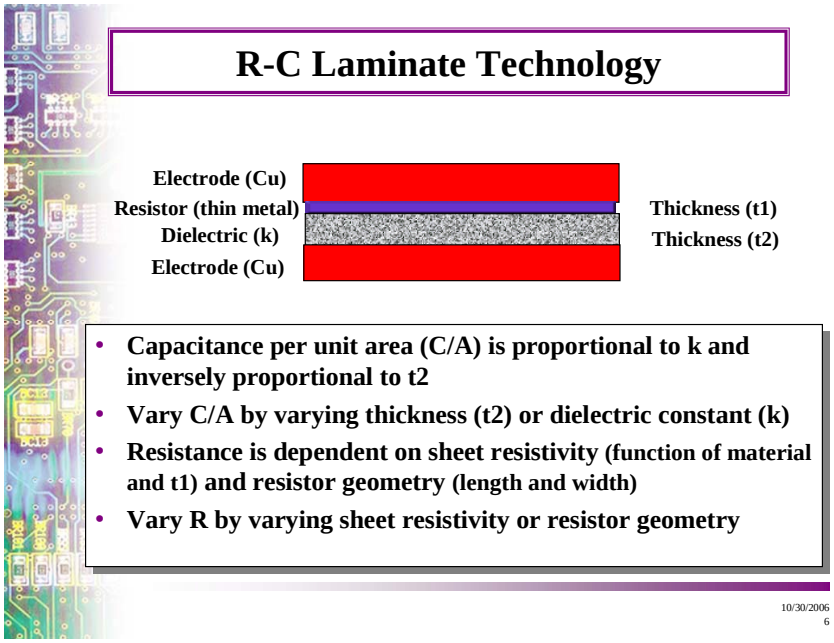

Figure 11 – R-C Laminate Technology

3M's embedded capacitor laminate materials have been actively sampled to fabricators and OEMs since 1998 to accelerate market adoption. This has been highly successful as much of the material presented in this paper came from pre-commercial sampling. These very positive electrical performance, EMI suppression, capacitor elimination and reliability results have led the way for the lead users to justify qualification of the product. Several OEMs have qualified the product and additional OEMs are currently in the qualification process.

Numerous market segments have strong interest in the ultra-thin embedded capacitor laminate materials. A pie chart shown in Figure 12 below indicates the activity level by market over the period of 2000 through mid-2006. As can be seen, the military/aerospace market accounts for one-third of the board builds over this time period. The telecom and computer/server markets have also shown a very strong interest in these materials. The portable market segment shows the lowest percentage of programs building builds to-date but this may change in the near future based on the very successful cell phone module program which ramped in 2006.

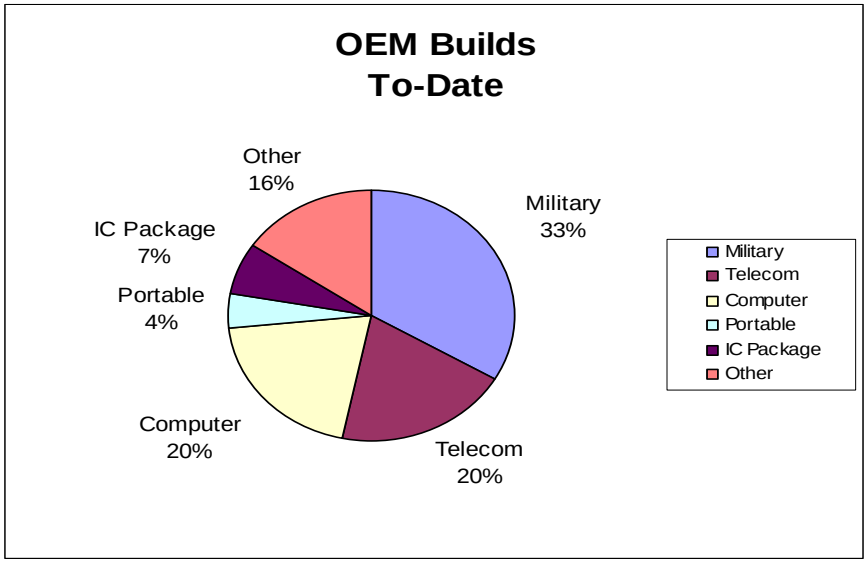

Figure 12 – OEM Board Builds by Market Segment

Over the last five to ten years, most of the industry interest has been in high speed digital designs where the embedded capacitance laminate material has been used in larger multilayer rigid boards. However, over the last couple of years interest and use of ultra-thin embedded capacitor laminate materials has increased in alternative products and applications such as chip packaging, modules, flex circuits and RF applications.

3M's high performance IC packaging facility in Eau Claire, WI has commercialized an IC package substrate with embedded capacitor material for the internal power-ground planes. This material is similar to the above-mentioned 14 um commercial material with a few exceptions, the major ones being that both the dielectric material and copper foil are thinner (8 um and 17 um respectively) and the capacitance density is over 10 nF/in^2.

One example of ultra-thin (8 um) embedded capacitance material (k of 16) being used in a flex circuit application is shown in Figure 13 below. Here an ~3" long two metal flex circuit utilizes the embedded capacitor material as the flex circuit substrate. The embedded capacitance material has a polyimide coverlay on each side and has had solder applied to the plated through holes.

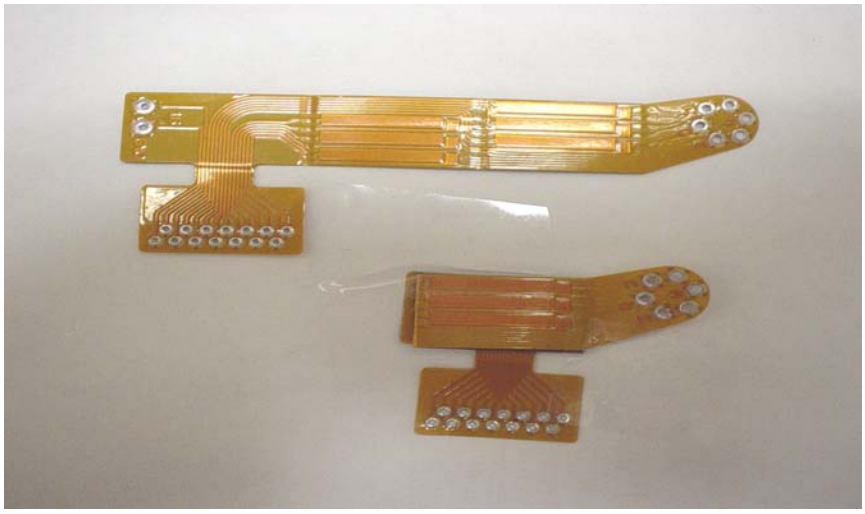

Figure 13 – Embedded Capacitor Substrate Used as a Flex Circuit

The embedded capacitor material has been patterned into circuit traces and 12 individual capacitors. Six of the capacitors are 330 pF transceiver and six are 33 pF receiver capacitors. The six pin flex is being qualified for use in commercial and military aircraft. The initial lot of circuits (10 parts/120 caps) all successfully passed a required 600 volt for 30 second high potential (hipot) test.

Summary

Embedded passives are of high interest today for OEMs looking to improve the electrical performance, reduce EMI, reduce the size, or lower the overall system cost of their products. Ultra-thin embedded capacitor materials with increased dielectric constants such as the 3M™ Embedded Capacitor Material can help OEMs achieve these objectives. The 3M material is commercially available, has short lead times and does not require a license from 3M. It has been used by over 60 printed board fabricators across the globe and has been shown to be manufacturable in high volume. Additionally, it has UL certification, is RoHS compliant and has shown that it is capable of meeting industry standard reliability tests including those for lead free assembly.

Acknowledgements

The author would like to thank the following individuals for providing input into this paper.

Bruce Archambeault – IBM
William Balliette – Formerly of 3M

John Grebenkemper – Hewlett-Packard
Bob Greenlee – Formerly of Merix
Todd Hubing – University of Missouri at Rolla
David Luenberg – 3M
Istvan Novak – Sun Microsystems

Portions of this paper were originally presented in May, 2006 at the IPC 3rd International Conference on Embedded Passives. It has been revised to show updated and additional information.

References

1. Joel S. Peiffer, "Using Embedded Capacitance to Improve Electrical Performance and Reduce Board Size", IPC 3rd International Conference on Embedded Passives, May 2006
2. Bruce Archambeault, Preliminary Test Data, 3M Embedded Capacitance vs. Typical Board, March 2005 (unpublished)
3. Joel S. Peiffer and William Balliette, "Decoupling of High Speed Digital Electronics with Embedded Capacitance", IMAPS ATW on Integrated Passives, January 2005
4. Joel S. Peiffer, "The History of Embedded Distributed Capacitance", Printed Circuit Design and Manufacture, August 2004
5. Joel S. Peiffer, "Impact of Embedded Capacitor Materials on Board Level Reliability", IPC 2nd International Conference on Embedded Passives, June 2004
6. Joel S. Peiffer, "Ultra-Thin, Loaded Epoxy Materials for Use as Embedded Capacitor Layers", Printed Circuit Design and Manufacture, April 2004
7 Advanced Embedded Passives Technology (AEPT) Program Report, September, 2003. National Center for Manufacturing Sciences, Ann Arbor, Michigan
8.. Joel S. Peiffer, "Ultra-Thin, Loaded Epoxy Materials for Use as Embedded Capacitor Layers", IPC International Conference on Embedded Passives, June 2003
9. Joel S. Peiffer, Bob Greenlee and Istvan Novak, "Electrical Performance Advantages of Ultra-Thin Dielectric Materials Used for Power-Ground Cores in High Speed, Multilayer Printed Circuit Boards", IPC Expo 2003 Proceedings, March 2003
10. M. Xu, T. Hubing, J. Chen, T. Van Doren, J. Drewniak and R. DuBroff, "Power-Bus Decoupling With Embedded Capacitance in Printed Circuit Board Design", IEEE Transactions on Electromagnetic Compatibility, Vol. 45, No. 1, February 2003
11. Joel S. Peiffer, NIST Advanced Embedded Passives Technology (AEPT) Industry Seminar, January, 2003
12. Bob Greenlee, "Processing Thin Core Capacitor Materials", IPC Expo 2002 Proceedings, March 2002
13. Embedded Decoupling Capacitance (EDC) Project Final Report, December, 2000. National Center for Manufacturing Sciences, Ann Arbor, Michigan