Embedded distributed capacitance is much older than most think, with the first known U.S. patents being issued in the 1920s. A look at six important — yet overlooked — works. by JOEL S. PEIFFER

Editor’s note: U.S. Patent 5,079,069, issued in January 1992 to James Howard and Greg Lucas and assigned to Zycon Corp., describes a concept known as “borrowed capacitance” on capacitive planes made of epoxy material of approximately 0.002” in thickness. The patent is currently owned by Sanmina-SCI.

Embedded distributed capacitance as a concept has been around since the 1920s, and was not invented in the late 1980s as some believe. In fact, embedded distributed capacitance and thin film nickel alloy resistors have been known in the art for many years. Both have been commercially practiced since at least the mid-1980s.

Certainly embedded passives, and specifically embedded capacitance, have been a hot topic over the past five years. During this time there have been at least two industry consortia1,2 on the topic, numerous presentations at technical conferences and a variety of trade journal publications3-10. The many advantages of embedded passives over traditional discrete technology in circuit boards and chip packages have been well documented in cited media. These advantages include improved electrical performance such as lower power bus noise and voltage ripple, reduced EMI, reduction in board size or layer count, removal of discrete components, cost reduction and improved reliability.

Embedded distributed capacitance is a rather simple concept. It involves using closely spaced power and ground planes as a parallel plate capacitor for power supply decoupling. Closely spaced power and ground planes provide significant capacitance and have very low inductance, ideal for power supply decoupling. This distributed embedded capacitance can also be used to replace discrete power supply decoupling capacitors from the board surface11. Further, the closely spaced planes provide very effective dampening of high-frequency noise on the planes.

FIGURE 1. A six-layer, epoxy-glass PCB with closely spaced power and ground planes was described in this 1983 filing.

FIGURE 2. The now infamous Leary patent, filed in 1982, describes a four-layer, epoxy-glass PCB with two copper voltage planes and two copper ground planes.
As mentioned, the concept of embedded distributed capacitance has been around since the 1920s. The following is a brief review of a number of patents that discuss and/or show examples of the concept of embedded distributed capacitance. This article focuses on U.S. patents only, although the concept of embedded distributed capacitance can also be found in other sources besides U.S. patent literature.

We begin with the most recent patent. U.S. Pat. No. 4,560,962 (“the ’962 patent”) was filed in 1983, issued to Michael Barrow in 1985, and assigned to Burroughs Corp. The ’962 patent describes a printed circuit board of six planar conductive layers separated by dielectric epoxy glass (FIGURE 1). The voltage (power) and ground planes are each one ounce (0.0014” or 35 µm) copper. The power plane is “separated from the ground plane by 0.005” of [epoxy-glass] substrate. This minimum separation ensures good voltage to ground noise decoupling.” The patent states that a “substrate of 5 mils is useful since the standard manufacturing practice is to provide a 5 mil separation between a ground plane and a voltage plane of conductive copper. However, this substrate thickness, normally standard for manufacturing, could be anywhere from 1 mil [25 µm] to 5 mils in thickness.”

U.S. Pat. No. 4,494,172 (“the ‘172 patent”), was filed in 1982, issued to Burton Leary, et al. in 1985, and assigned to Mupac Corp.12,13. The ‘172 patent describes a multilayer panel board with two copper voltage plates and two copper ground plates separated from each other by a layer of glass epoxy (FIGURE 2). One of the voltage plates is located between the two ground plates. The epoxy layers between the voltage plate and ground plates are “between about 0.005 inches and about 0.009 inches” thick “to establish a large distributed capacitance of about 0.03 microfarads between the voltage plate and ground plates.” The patent further states that “the close spacing of a voltage layer between two ground layers provides a large distributed capacitance (without requiring many discrete isolation capacitors) which inhibits switching
signals from causing voltage spikes in the power lines [power bus noise].” Mupac shipped millions of dollars of wire-wrap boards using the Leary construction prior to 1989.12,14

U.S. Pat. No. 4,004,196 (“the ‘196 patent”), was filed in 1975, issued to Leonard A. Doucet in 1977, and assigned to Augat Inc. The ‘196 patent describes a multilayer panel board having three voltage planes in combination with one or more single-in-line package (SIP) termination resistor networks. The voltage planes are separated by conventional insulating board such as glass epoxy. One voltage plane is used for ground. The ‘196 patent states that “all of the voltage planes provide low impedance power distribution. The capacitance between each voltage plane is about 1,000 pF for a DIP panel, enough to provide a low-noise reference plane for most applications.” The patent goes on to state: “If desired, one of the voltage planes could be separated into two independent adjacent areas [split power plane] to provide yet a fourth bus.”

U.S. Pat. No. 3,519,959 (“the ‘959 patent”) was filed in 1966 (with a continuation-in-part filed in 1969), issued to Lawrence L. Bewley, et al. in 1970, and was assigned to Burroughs Corp. The ‘959 patent describes an electrical signal distribution network, which can include two layers of embedded distributed capacitance (see, e.g., FIGURE 3). The patent describes a “conductive sheet having a direct current voltage applied there-to [that] is sandwiched between a pair of thin dielectric sheets having a high dielectric constant. These sheets are sandwiched between two additional conductive sheets that are maintained at ground potential. The resulting active voltage sheet is characterized by a low impedance and high capacity to ground. Noise spikes resulting from switching or other electrical disturbances in components drawing power from this active plane are grounded by the high capacity and an improved noise level and component performance results from this invention.”

The ‘959 patent also states that “the conductive sheets may be any suitable conductive material such as copper, silver or gold. The dielectric sheets may be any suitable dielectric such as epoxy glass.” The patent goes on to say that “the dielectric sheets for the distribution network of this invention can be selected from materials having known dielectric constants. By varying the thickness of the dielectric sheets...
having a desired dielectric constant, the inductance for the network is control-
lably decreased and the capacitance for
the network is controllably increased.”

Finally, the ‘959 patent states that the current carrying sheet “may be a
two ounce copper sheet approximately .0025 inch thick” and that “epoxy
glass sheets may have a dielectric con-
stant of 4 and are also approximately .0025 inch thick.”

U.S. Pat. No. 3,312,870 (“the ‘870
patent”), was filed in 1964, issued to
William T. Rhoades in 1967, and
assigned to Hughes Aircraft Co. The
‘870 patent states that an object of the
invention is “to provide an electrical
transmission system which minimizes
the transmission of transient electrical
fluctuations” (power bus noise) such as
those caused by simultaneously switch-
ing of electronic circuits in complex
electronic equipment such as comput-
ers. The patent also states that “another
object of the invention is the provision
of an electrical transmission system hav-
ing an extremely low impedance.”

The ‘870 invention accomplishes
these objectives by having “an electrical
transmission line formed of three elong-
gated conductive plates having insulated
outer surfaces. The plates are arranged
with their broad surfaces substantially
coeffective, parallel and adjacent to
form a laminated structure. The inner
plate is used as the current path for con-
duction in one direction and the return
path is by way of the two outer plates in
parallel.” (See FIGURE 4.) The conduc-
tive plates in the example are made of
aluminum alloy but the patent states
that electrical conductors other than
aluminum can also be used.

The ‘870 patent goes on to explain
that “placing the cur-
rent path as
close as possible
returns path reduces the effective inductance
of the transmission line by cancellation of
the inductive field. Hence, the insulating
films are made as thin as is feasible.” The patent explains that this can
be accomplished by anodizing the al-
uminum plates to a depth of 0.0005” and
laminating them together under heat
and pressure with an epoxy resin. In
this case, the epoxy resin is only
0.002” or less in thickness. The patent
continues with: “To decrease the capac-
tance reactance of the transmission
line, the capacitance between the plates
is made as high as possible.” This is
accomplished by keeping the insulation
layer as thin as possible and by further
adding a “loading” material to the
adhesive. In this case, aluminum oxide
powder on the order of 350 to 450
mesh was used, which increased the
dielectric constant of the adhesive to
30. This provided a transmission line
with a capacitance of 300 nanofarads
per foot in length and a characteristic
impedance of 0.05Ω (500 million).

The ‘870 patent goes on to explain
that when computers used conventional
wiring instead of the transmission lines of
the invention, the speed of the gate
circuits is in the range of 500 - 1000
nanoseconds. When a transmission line
of the invention was used to distribute
power to the circuit board, the speed of
the gates was approximately 20
nanoseconds. When a different embed-
ment of the transmission line was used,
the speed of the gates was on the order
of about one nanosecond.

Finally, U.S. Pat. No. 1,999,137
(“the ‘137 patent”), filed in 1926,
issued to Edmund T. Flewelling in
1935, and assigned to Frank L. Walker,
sought to bypass high-frequency cur-
rents and to simplify wiring – pri-
marily for radio apparatus. The ‘137 patent
describes a “combined [power] distrib-
utor and condenser [capacitor] strip
consisting of a plurality of separate
electrical conductors arranged in paral-
lel spaced relation, and preferably in a
body of dielectric or insulating materi-
al.” (See FIGURE 5.)

The ‘137 patent goes on to state that
“the multiconductors are prefer-
ably thin flat strips of sheet metal” and
that “these metallic conductor strips
are separated one from another by
interposed strips of fabric impregnated
with phenolic condensation material or
other material possessing insulating
and dielectric properties. The assembly
is then permanently united, preferably
though not necessary, under the influ-
ence of heat and pressure to form a
unitary strip or body in which the con-
ductor strips are fixedly embedded in
parallel spaced relation.”

The ‘137 patent recognized that this
method of “electrical distribution,” in
addition to being useful for device
mounting, power distribution and sim-
plified wiring, was most important for capacitive effects by the statement: “The convenience of this multi-conductor strip for distribution of electrical current ... is, however, more or less subordinate to the intercapacitance electrical effect afforded by the superposed spaced conductor strips which form a fixed by-pass condenser for all alternating currents whether radio or audio frequency.”

In summary, the above six U.S. patents clearly demonstrate several facts about the history of embedded distributed capacitance:

■ The concept of intercapacity electrical effect of metallic conductor strips interposed with dielectric materials for use in electronics dates to at least 1926 (U.S. Pat. No. 1,999,137).
■ The concept of using power and ground planes in printed circuit boards has been in the public domain for almost 40 years (U.S. Pat. No. 3,312,870).
■ The concept of using very thin epoxy glass (approximately 0.0025”) between copper power and ground planes in multilayer printed circuit boards, very similar to what is done in high volume today, goes back to at least the late 1960s (U.S. Pat. No. 3,519,959).
■ The concept of using dielectric spacing below 0.002” between the power and ground planes in an epoxy glass multilayer printed circuit board is at least 20 years old (U.S. Pat. No. 4,560,962).

Thus, the notion that embedded distributed capacitance was invented in the late 1980s is greatly mistaken. The concept of distributed embedded capacitance for use in printed circuit boards has been known for almost 40 years.

REFERENCES
1. NCMS Embedded Decoupling Capacitance (EDC) Project.
2. NIST Advanced Embedded Passives Technology (AEPT) Project.

JOEL S. PEIFFER is an applications engineering specialist in the Corporate Research Materials Laboratory, 3M Co. (mmm.com). He can be reached at jspeiffer@mmm.com.