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Heat Resistant Bump Protection Tape with Easy Debonding

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Abstract

This paper presents a novel high temperature tape developed to support the wafer level package process. The high temperature resistant backing film with cross linkable adhesive was designed to fit the die to wafer or package-on-package process. With high initial adhesion for robust bumped wafer support, excellent thermal stability to carry the fan out or interposer wafer through the die stacking steps and resist reflow with easy final debonding of the tape. The adhesive was designed for clean removal on metal pads or solder bump surfaces, meeting the requirements for HVM (high volume mass production).

In this article, we demonstrate the tape can be easily attached on a metal frame as a supporting tape carrier, then laminated with the device wafer to provide uniform bump coverage, with proper adhesion strength and adhesive modulus and thickness design, no delamination or rebound occurs after wafer lamination. To address the challenges, including high temp resistance; bump protection; tape release and residue concerns, key process conditions were simulated to evaluate the tape's performance.

The demonstration of tape performance in these critical process conditions, designed to simulate advanced packaging process steps and key quality attributes, shows that the newly developed advanced package process tape can fully support the wide range of processes needed for better performance in the semiconductor advanced packaging industry.

Key Words: Die to Wafer; Package on Package; High Temp Process Tape; Wafer Level Package; Fan out Package.

I. Introduction

2.5D/3D heterogeneous packaging has enabled high-performance package technologies to achieve increased circuit densities, enhanced band width, and lower power consumption. Many process variants have been developed by Fabs and OSATs, for example, integrated fan out (InFO from TSMC); fanout chip on substrate package (FOCoS from ASE); chip on wafer on substrate (CoWoS from TSMC) and Foveros / EMIB from Intel. Those designs unveil the concept of system on chip (SOC) though chip to wafer or package on package 2.5D / 3D package technology. To support the wafer level package process, temporary bonding / debonding (TBDB) of carriers has been developed over a number of years to improve handling of thin and fragile substrates. Within fan out packaging, UHD FO (Ultra High Density Fan Out) is experiencing the highest growth rate at CAGR 20.7% for high end applications like networking and HPC. The technology trend for fan out has been towards a higher integration level, as FOWLP enables many integration possibilities including PoP, SiP or MCM.

Various multi-stack fan out packaging formats are expected to achieve higher memory capacity and bandwidth. However, total cost reduction and process yield improvement has been one of the roadblocks to

grow fan out into a bigger platform. The overall cost can be relatively high compared with a carrier-less process, for example, using tape to support the backend package process.

II. Application and Performance Challenge

i. Process for Die to Wafer Package

A demonstration of the high temperature performance of this tape starts from target wafer attach onto the tape. The tape can be handled in frame format using a standard roll type laminator, in a similar manner as a dicing tape process. The laminator can easily laminate the tape to the metal frame. See Fig.1(a). After frame attach, the wafer form package is bonded to the tape by vacuum compression to achieve good uniformity and TTV level. The wafer form package could comprise a variety of wafer types, for example, an interposer wafer; TSV wafer; fan out OS (on substrate) package with bumps or pads on the wafer top side. See Fig. 1(b).

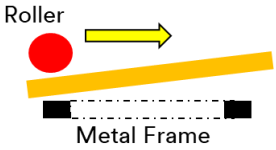

Fig. 1(a), the tape can easily be laminated to the metal frame by a laminator

Fig. 1(b), the wafer form package bonds to the tape after frame attach

The tape adhesive may be fully covered with bumps/pads or partially covered, depending on wafer format and the adhesive thickness design. The assembly could follow a die to wafer or wafer to wafer bonding process, with pre-tack and reflow processes. See Fig. 2.

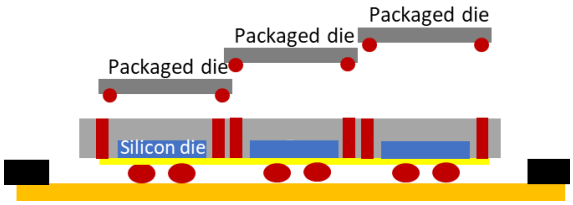

Fig. 2, D2W, W2W with pre-tack and reflow processes can be done with bumps covered by the tape

This tape was designed for high temperature resistance and can withstand 200°C / 2 hr exposure to fulfill various packaging material and process requirements.

ii. Product Design and Feature

The primary application for this process tape is to support the wafer format package through several necessary high temperature process steps. The adhesive was designed to have a thermal debond function along with robust resistance to high process temperatures and durations. See Fig. 3. The tape structure is shown in Fig. 4. The adhesive thickness was targeted to 20-60 µm to meet the requirements of various types of I/O connections. The high temperature resistant backing film is normally polyimide, but other temperature resistant films which meet specific process temperature requirements may also be an option.

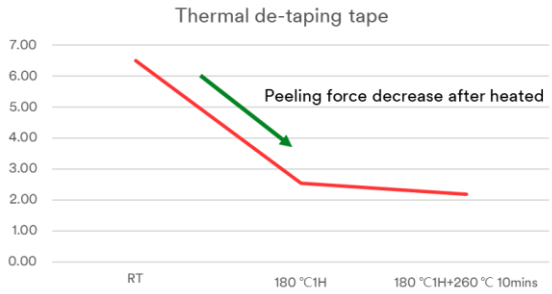

Fig. 3, the adhesive is designed with a thermal debond function

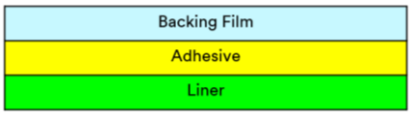

Fig. 4, the structure of the tape

The adhesive crosslink density must be carefully designed to meet the process requirements for peel strength and residue. The adhesive peel strength is inversely proportional to adhesive crosslink density. When the adhesive has higher crosslink density, the adhesion is decreased. On the other hand, the adhesive modulus and cohesion increases with crosslink density. These properties must be balanced to achieve the required adhesion through processing, release without damage to pads or solder bumps, and clean, residue free removal. See Fig. 5.

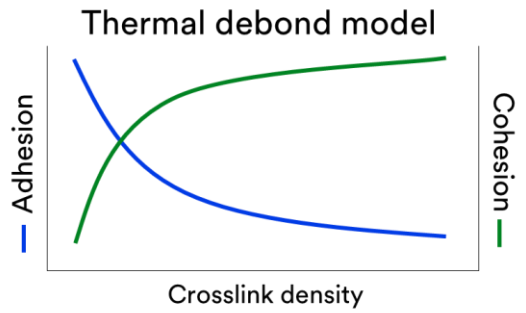

Fig. 5, the adhesive modulus and cohesion are designed to achieve the required adhesion through multiple processes

iii. Package Process Condition Simulation

Simulation of processes requiring higher temperatures in the advanced packaging process was carried out to understand the tape performance and critical challenges of the application. A high temperature 180°C /1 hr + 260°C / 10 min bake step was performed to simulate various processes such as sputtering, molding, plasma clean and die attach and the final solder reflow step. Fig. 6(a) depicts the test set-up, with tape performance checked in the key process challenges of adhesion, residue and bump damage as shown in Figures 6(b)-(d).

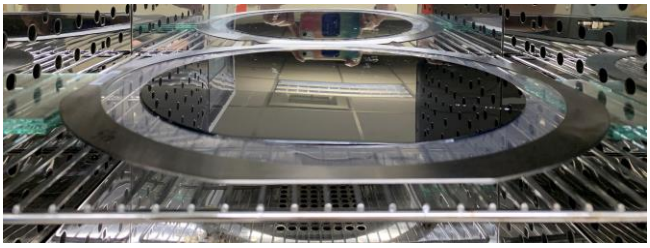

Fig.6 (a), Metal frame was set for suspension at 10 mm height

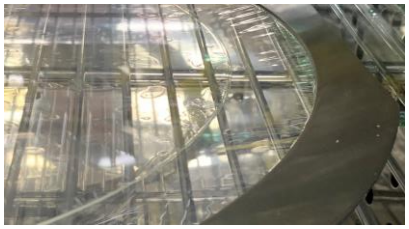

Fig.6 (b), thermal detach in adhesive

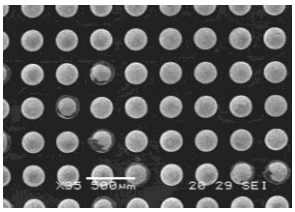

Fig.6 (c), Residue check

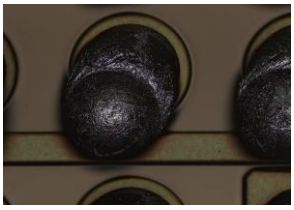

Fig.6 (d), Bump damage check

Table 1 shows pre- and post- thermal exposure adhesion strength testing, which was performed to demonstrate the tape's thermal stability and peel force reduction after high temperature processing. This property of the tape results in sufficient adhesive strength during processing to maintain adhesion to the wafer and frame but allows for easy debonding performance. The tape is also compatible with two solder reflow cycles at 260°C for 10 minutes without adhesive degradation or risk of tape breakage. This performance provides for the possibility of applications requiring a 2nd layer die stack, with more chip functionality to align with recent heterogenous package technology trends.

Table 1, Tape adhesion with temperature simulation

Peeling Force			
Item	RT	180°C/1H+260°C/10Mins	180°C/1H+260°C/10Mins X 2 cycles
3M HT process tape	7.08	1.82	1.69
*condition: width: 2.54cm \ time: 20mins \ unit: N \ substrate: SUS			

After the high temperature process treatments, the tape was easily removed without bump damage, as evident through high magnification microscopic inspection. The tape's debonding performance can significantly reduce the yield loss and achieve cost reduction for very backend SOC package chip sets. See Fig. 7.

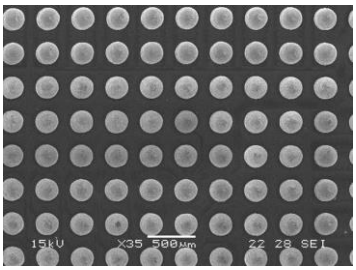

Fig. 7, Residue inspection after tape removal

To understand the performance of the tape in protection of solder bumps during processing, several adhesive formulation DOEs were conducted, making use of the same high temperature process conditions cited previously. In evaluating formulations at targeted levels of adhesive crosslinking, it was demonstrated that the crosslink density correlates strongly with the relative amount of bump damage or distortion. See Fig. 8. The adhesive becomes stronger as the crosslink density is increased, providing better support to bumps when solder balls soften and melt when at or near the reflow temperature.

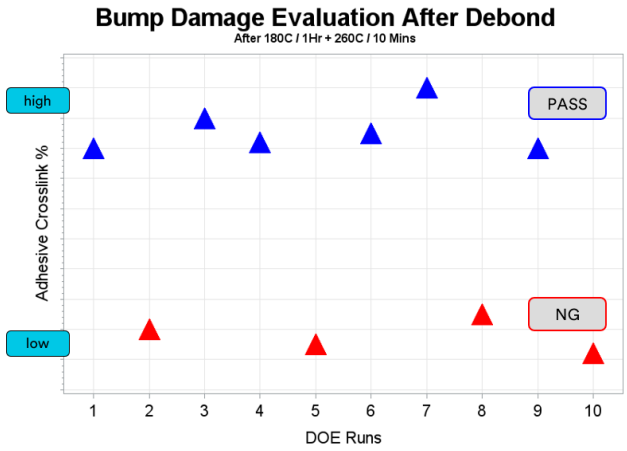

Fig. 8, Bump damage evaluation

III. Conclusion

A newly designed high temperature process tape has been presented. The product shows excellent wafer support performance as demonstrated through simulation of several high temperature and high loading process conditions. Various tape thickness designs can meet different wafer surface structure requirements, which include solder bumps, C4 bumps, micro bumps and pads, and other I/O connection needs. With proper adhesive formulation design and crosslink density control, the tape adhesive can achieve high initial adhesion, but allow lower detaping strength after thermal processing, thus minimizing or eliminating bump damage and residue.

Acknowledgments

The authors wish to thank Joann Wang, and all our coworkers who have assisted in the development and testing of the high temperature process tape.

References

[1] S. Kumar, S. Chitoraga, F. Shoo, "Status of the advanced packaging industry 2021", Yole Développement Market and Technology Report, 2021, pp. 117-149.

[2] W. Shen, Y. Lin, S. Chen, H. Chang, T. Change, W. Lo, C. Lin, "3-D Stacked Technology of DRAM-Logic Controller Using Through-Silicon Via (TSV)", Journal of the Electronic Devices Society, pp. 396-402, Volume 6, 2018.

[3] M.J. Zajaczkowski, "Pressure sensitive adhesives in high performance applications", The Adhesives and Sealants Council, Inc., 2010.

[4] D. J. McClure, "Polyimide Film As a Vacuum Coating Substrate", 53rd SVC Technical Conference, 2010.

[5] Y. Arimitsu, T. Oshima, A. Murata, K. Kiuchi, "Thermal release sheet 'Revalpha'", Nitto Technical Report, Volume 36, 1998, pp. 52-53.

[6] D. Wilson, H.D. Stenzenberger, P.M Hergenrother, B. Glasgow, "Polyimides", ISBN 0-412-02181-1, 1990.

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