Valerie St.Cyr is the Supply Base Development Manager for Printed Circuit Boards and Backplanes for Sun Microsystems. She has been with Sun for 3 years in technology development, new product introduction, and supply chain management roles. Prior to joining Sun, Valerie was with Digital Equipment Corp. for 10 years where she was a Principal Manufacturing Engineer responsible for VAX systems’ PCBs, and later the Acquisition Program Manager for Digital’s StorageWorks line. Before that Valerie worked in the industry for over 12 years having departmental management responsibility for materials, lamination, mechanical CNC operations, and soldermask. Valerie holds a degree in Business Management and is a Certified Purchasing Manager (National Association of Purchasing Management). valerie.st.cyr@sun.com, (tel): 781-442-0982

Istvan Novak is signal-integrity senior staff engineer at SUN Microsystems, Inc. Besides of signal-integrity verification of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks, bypassing and decoupling of packages and printed-circuit boards for workgroup servers. He creates simulation models, and develops measurement techniques for power-distribution networks. Istvan has more than twenty years of experience with high-speed digital, RF, and analog circuit and system design. He is Fellow of IEEE for his contributions to the signal-integrity and RF measurement and simulation methodologies. Istvan holds a masters degree and PhD in Electrical Engineering. istvan.novak@sun.com, (tel): 781-442-0340

Current applications with <= .002" P/G cores:
Yes

Key driver(s):
Reducing dl/dt noise on power planes

Nominal dimensions and tolerances:
see below

Benefits:
Reduced noise across planes due to lower plane inductance,
reduced radiation,
reduced overall board thickness

Any active (very, ultra, extremely) thin core projects? Yes
Describe:
Very thin (.001” cores) being tested in current production parts
Ultra Thin (.0003” cores) have very limited engineering part samples
eXtremely Thin (.00003") have lab samples

Key driver(s):
same as above

Perceived benefits:
same as above, plus
reducing/eliminating plane resonances

Constraints to implementation:
modeling and verification data
availability;
cost (raw materials)
cost (fabricated)

Dielectric Strength (Withstanding Voltage) Requirement?
250V/mil
Cost budget or tolerance for cost premium:
  modest cost premium as an early adopter
  expecting cost/value parity after not more than 2 yrs.

Alternatives:
  Use different system partitioning to reduce the amount of high-speed current entering the PCB planes: reduce current/line, reduce number of lines simultaneously switching, increase transition time, divert current from entering PCB planes by using capacitors on silicon and/or package

List desired physical attributes:
  large panel form (=> 18 x 24")
  copper clad thickness options
  thickness range one-sided: thickness not to exceed .001" etc.

List desired electrical attributes:
  Low inductance,
  resonance-free self-impedance,
  low-pass transfer impedance

If available, within cost budget, use would be: Pervasive

Schedule; desired time to:

<table>
<thead>
<tr>
<th></th>
<th>.001&quot;</th>
<th>.0003&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Samples / Eng/ Verification:</td>
<td>Now</td>
<td>Now</td>
</tr>
<tr>
<td>Proto-Circuits:</td>
<td>Now</td>
<td>6 - 9 months</td>
</tr>
<tr>
<td>Volume Circuits:</td>
<td>6 months</td>
<td>12 - 15 months</td>
</tr>
</tbody>
</table>

**Thin Laminate Electrical Benefits**

- Inductance (L) is proportional to thickness (t)
- dV=L*dl/dt: SSN is less if L is lower
- Plane resonances are suppressed if t<0.3 mils
- Low-pass noise propagation if t<1um
- Radiation is less from thinner laminates
- Dielectric constant increases static capacitance, but L is unchanged
Resonance-Free Planes for $t<0.3\text{mils}$

Magnitude of self impedance at center [ohm]

10"x10" planes
Bare board
Simulated, $t=$
- 10-mil
- 5-mil
- 2-mil
- 1-mil
- 0.5-mil
- 0.2-mil
- 0.1-mil
- 0.05-mil
- 0.02-mil
- 0.01-mil

Low-pass Transfer for $t<1\text{um}$

Magnitude of transfer impedance corner-to-center [ohm]

10"x10" planes
Bare board
Simulated, $t=$
- 10-mil
- 5-mil
- 2-mil
- 1-mil
- 0.5-mil
- 0.2-mil
- 0.1-mil
- 0.05-mil (1.2um)
- 0.02-mil
- 0.01-mil
10”x5” Test Board

Measured Self Impedance

![Graph showing measured self impedance for different layer thicknesses (2 mil, 1 mil, 0.3 mil) and bare board with frequency range from 10^6 Hz to 10^9 Hz and impedance magnitude from 10^0 ohm to 10^9 ohm.](image)
Measured Close-Field Radiation

- Relative radiation field [dB]
- Frequency [Hz]
- 2 mil, 1 mil, 0.3 mil
- Bare board

Impedance on Small Board
Geometry

- Paralleled plane pairs
- Bare board
- Same construction, with
  - Aromat 2-mil FR4 BC2000
  - DuPont 1-mil HiK
  - Aromat 1-mil FR4
  - 3M 0.3-mil C-Ply
Impedance on Small Board
Self-impedance at (1)

<table>
<thead>
<tr>
<th>Frequency [Hz]</th>
<th>ZBC2000</th>
<th>Dup-HikI</th>
<th>1-mil FR4</th>
<th>C-Ply</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.E-04</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E-03</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E-02</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+00</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+02</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+03</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+04</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+05</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+06</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+07</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+08</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+09</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
<tr>
<td>1.E+10</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
<td>1.0E-01</td>
</tr>
</tbody>
</table>

Impedance on Small Board
Transfer-impedance (2)