Presented at IPC Printed Circuits EXPO® 2001
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Fabrication of Embedded Capacitance Printed Circuit Boards

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Abstract
Embedding capacitor materials into printed circuit boards or electronic packages offers many benefits. These include improved electrical performance, increased packaging density, improved reliability and potential cost reduction. Boards made with very thin embedded capacitor materials that have high capacitance and very low inductance have been shown to improve signal integrity, reduce power bus noise and reduce EMI. This is especially true at higher frequencies where discrete capacitors lose their effectiveness (~500 MHz+). Replacement of surface mounted discrete capacitors with an embedded capacitor layer allows for tighter component spacing, reduced via count and increased routing area. This could allow for a reduction in the board size and/or board layers or a reduction in the total number of boards required per system. An improvement in system reliability is likely since there would be a reduction in the number of solder joints and vias. When the above benefits are coupled with a reduction in the costs of the capacitors, their placement (and rework), the overall goal of a more reliable, better performing, cost-effective capacitor material should be the result.

However, the above mentioned improvements in electrical performance, reliability, space reduction, and cost-effectiveness will only be realized by the OEM if the printed circuit board (PCB) fabricator can produce quality product in a production environment in a timely manner. This paper will show that PCB fabricators have made quality embedded capacitor PCB's on a prototype basis, which should be extendable to a production basis in the future.

Background
3M has been working very aggressively on embedded capacitor materials since the mid-90's. This work has included a DARPA program (Planar Capacitor Layer for Mixed Signal MCM's) and membership in consortia on embedded capacitance for power supply decoupling (NCMS Embedded Distributive Capacitance Project) and embedded passives (NCMS/NIST ATP Advanced Passives Technology Consortium). A number of printed circuit boards, both rigid and flex, were fabricated with 3M C-Ply embedded capacitor material for the above mentioned programs to determine PCB process compatibility, environmental testing and measurement of electrical performance. A number of boards have been also fabricated for OEMs outside of these consortia for the same reasons. In total, over 12 different PCB designs have been fabricated to-date. These boards have been fabricated internally as well as at four domestic printed circuit board fabricators.

Introduction
This paper will focus what has been learned from design and fabrication of the many embedded capacitor test vehicles from numerous fabricators. This information should be of great benefit to potential PCB fabricators of embedded capacitance materials. It will also be helpful to OEMs who will need to design the board and specify the proper material. Prior to reviewing this information, it will be beneficial to understand what an embedded capacitor looks like, as well as its general material and electrical properties.

Many embedded capacitor materials for printed circuit boards are laminates in which the dielectric is clad with copper on both sides. The dielectric is typically epoxy or polyimide-based and is often loaded with a high dielectric constant ceramic filler to increase capacitance. The dielectric thickness is usually kept as thin as possible to increase capacitance and more importantly, decrease inductance. In the case of this embedded capacitor material, the dielectric is epoxy-based, loaded with barium titanate and is extremely thin. The dielectric is clad on both sides with one-ounce copper (typically). Some of its basic material and electrical properties are shown below:

- Dielectric Material: Epoxy (non-brominated) filled with $BaTiO_3$ particles
- Dielectric Thickness: 0.15 – 1.00 mil (4 – 25 um)
- Copper Thickness: 0.7 mils – 2.8 mils (1.4 mil (one-ounce) standard)
- Dielectric Constant: 14 – 18 (dependent on amount of $BaTiO_3$ loading)
- Capacitance: 5 – 30 nF/in^2 (at 25°C and 1 kHz)
- Capacitance Uniformity: ± 5%
- Dissipation Factor: 0.005 (at 25°C and 1 kHz)
- Frequency: Performs well to at least 5 GHz*
- Operating Temperature: -40°C to 125°C ("X7R" behavior over this range)
- Adhesion: > 4 pounds per inch

*2-3% decrease in capacitance per frequency decade (above 100KHz)

The non-reinforced dielectric and flexibility of the material does require some minor design and material handling procedures compared to a standard rigid board (FR-4) process. The epoxy-based dielectric can be processed almost identically to the fabricator's typical FR-4 material as far as process sequence, process chemistries and process parameters (time, temperature, concentrations, etc.) for each step without any process or quality issues. It should be noted that this embedded capacitor material does not have any metal tie layers or adhesion promoters which require specific or additional process steps or chemistries. The design and fabrication this embedded capacitor PCBs is summarized in detail below.

Phototool Design

The embedded capacitor dielectric is very thin and not self-supporting. This necessitates the need for a set of design guidelines for material handling purposes. Below are the guidelines for using this material as a distributive capacitance layer (power/ground) in printed circuit boards when both sides of the copper are patterned at the same time (i.e. no sequential lamination).

1. One of the copper layers (typically ground) will need to be extended to the panel edges. This will leave exposed copper at the board edges following routing. It is recommended that the copper at the board edges be electrically isolated from the active board area by using a small copper cut out (space) surrounding the active board area.

2. Leave as much copper on the panel as possible for mechanical strength. Copper should only be removed where it is necessary (clearance holes, through-holes, tooling holes, etc.). If venting is used for lamination, keep the slot width as small as possible and the slots as far apart as possible.

3. If split power and/or ground planes are used, the isolation spacing should be kept as small as possible for mechanical strength. However, avoid the use of long, narrow, straight copper cut outs since they make an ideal location for creasing.

4. Large areas (> 0.250 inch in either direction) of copper must not be removed from opposing sides of the panel in the same location. This will minimize the potential for mechanical damage during material handling and processing.

5. When large sized areas (one > 0.250 inch) of copper must be removed from opposing sides of the panel in the same general area, a minimum of 0.250 inch (and preferably 0.500 inch) distance (edge-to-edge) should be left between them.

NOTE: If sequential lamination is used (one side patterned and laminated prior to patterning second side), there are NO design restrictions and none of the above design rules are required

Board Stack-Up Design

The embedded capacitor layer can be placed anywhere in the board stack up (including outer layers if desired). Multiple layers can be used to increase capacitance and lower inductance. Placing the embedded capacitor layer closer to the surface (closer to the IC's) will reduce via inductance and make the capacitor material more effective, especially at high frequencies. If more than one embedded capacitor layer is used, they should be distributed so there is a balanced stack-up so board warping is kept to a minimum.

Material Handling

The embedded capacitor laminate has a thin, non-reinforced dielectric layer that is clad with one-ounce copper on each side. The material is flexible and derives most of its stiffness from the copper foil. Material handling of the laminate is similar to handling two-ounce copper foil. This typically necessitates special material handling for most conveyorized processing prior to lamination. One fabricator who has "thin core" processing equipment found they did not need special material handling processes when they used a sequential lamination process. The handling procedures used by most fabricators included leaders, carrier panels or "picture-frame" carriers. Once the embedded capacitor material was laminated into the multilayer board, all fabricators utilized standard material handling.

Process Compatibility

As previously mentioned, over 12 board designs have been built with embedded capacitance. These have ranged from 4 to 20 layers and have used up to four layers of embedded capacitor material per board. Both rigid (FR-4) and flex (polyimide) boards have been produced although this paper will focus on rigid board fabrication. The five different fabricators used very similar fabrication methods for the most part. The largest difference in processing is due to some fabricators preferring to use a sequential lamination process for patterning of the embedded capacitor material, whereas other fabricators chose to pattern both sides at once. (The sequential lamination process reduces material handling issues, eliminates any design restrictions and leaves no exposed copper at the board edges). Any known deviations from typical FR-4 processing by any fabricator have been noted.

Inner Layer/Oxide (Standard Inner Layer Process)
Standard processing speeds, materials and chemistry were used for wet chemical clean, aqueous dry film lamination, UV expose and develop, etch and strip (DES). Both acid and ammoniacal cupric chloride etchants were used. Post-etch-punch was utilized by the fabricators who had that capability. Standard oxide processes were used by all fabricators (most used reduced oxide). The dielectric material is compatible with all inner layer processing. One slight change was that resist must be brought out to the panel edges on at least one side of the panel ("no postage stamping"). There is also potential for dielectric "blow-out" on very thin dielectric where copper has been removed on both sides in the same area. Special material handling was used by all fabricators for wet chemical clean and DES.

Inner Layer/Oxide (Sequential Lamination Process)
Some of the board fabricators already used sequential lamination processes for microvia boards so this was a process already familiar to them. The sequential lamination process for embedded capacitor material consists of patterning one side of the embedded capacitor material, laminating the patterned side to pre-preg as a carrier and then patterning the other side of the material. Thus, the amount of inner layer processing is essentially doubled. However, most fabricators have found that this is more than offset by the elimination of design restrictions, the reduction of material handling issues, elimination of dielectric "blow-out", the need to bring resist to the board edges and no exposed copper at the board edges.

Automated Optical Inspection (AOI)
Most fabricators did not use AOI since most designs were test vehicles and/or power/ground cores. However, the fabricators who did AOI embedded capacitor cores had no issues.

Electrical Test (HiPot)
Embedded capacitor material can be tested for insulation resistance similar to other cores. However, the capacitor material will charge during the test. Measurement of the insulation resistance must not occur until after the capacitor material has fully charged, otherwise the tester will measure the charging current and may indicate a failure. The panel should be discharged prior to being removed from the tester. Since the dielectric material is much thinner than standard core material, any small material defects have the potential to significantly affect insulation resistance. Depending on the dielectric thickness and design, the testing voltage was from 50V to 500V (250V maximum preferred). One fabricator was able to measure the capacitance and dissipation factor (loss tangent) with slight modifications to the tester (this can also be done at final e-test if desired). Known good material was not sent to fabricators so there was some yield loss at this step. In the case of sequential lamination, the panels must be measured after the first patterning process (there is no electrical access to first-patterned side after lamination).

Lamination
Care must be used in the lay-up of embedded capacitor material (especially when a non-sequential lamination process is used). The material can be stretched over fixture pins if the proper procedure is not followed. For fabricators who are used to using bare copper foil in lay-ups, this would be nothing new. For sequential lamination sub-parts, there are no material handling issues. Standard FR-4 lamination times, temperatures and pressures were used by all fabricators (typically high Tg FR-4). Scaling factors for non-reinforced embedded capacitor material will be different than for FR-4. If sequential lamination is used, each side will likely have a different scaling factor.

Drill/Through-Hole/Laser Ablation
Standard FR-4 drill parameters were used (speeds, feeds, etc.) by all fabricators. Since the embedded capacitor material is thin and contains extremely small $BaTiO_3$ particles, no effect on drill life is anticipated. All fabricators used wet chemical desmear/electroless copper for etchback and metallization (several different vendors' chemistries were used). Each fabricator used their standard FR-4 process. The embedded capacitor material was fully compatible with drill and through-hole processing. Several boards with laser ablated vias (UV-YAG; 355 nm) were made without any issues. It should be noted that ceramic loaded dielectric material is not compatible with plasma desmear since the $BaTiO_3$ particles tend to mask the epoxy from the plasma.

Outer Layer
Standard FR-4 processing was used for outer layer imaging, plating, patterning and solder mask at all fabricators. There were no process issues for any fabricator.

Surface Finish/Rout
All designs either used organic solderability preservative (OSP) or Hot Air Solder Level (HASL). Standard FR-4 processing was used by all fabricators. Some fabricators used a slightly longer pre-HASL bake to ensure all moisture was removed from the embedded capacitor layer. There were no surface finish process issues for any fabricator. There were also no issues with routing although it should be noted that fabricators who chose to use non-sequential lamination will be routing through copper on one layer of the embedded capacitor material.

Final Inspection/E-Test

There have been no issues due to the embedded capacitor material at final inspection or final e-test (continuity and insulation resistance). There were no e-test failures due to the embedded capacitor material. If there were defects in the incoming embedded capacitor material, in every case, it was caught at inner layer HiPot test. No defects were created in the fabrication process. There was no change in the capacitance or dissipation factor of the material after fabrication. The lone case where there were final e-test failures (shorting) it was due to misregistration of the embedded capacitor material. This was on an initial lot of a tight registration design (drill + 16 mil) on an 18" X 24" panel and was before the fabricator had material scaling factors determined for their process. Once the scaling factors were determined, the board was fabricated without any registration issues.

Cross-Sections/Reliability Testing

Many cross-sections have been taken from finished boards (see Figure 1). In every case, there has been no evidence of post-separation, voiding, hole-wall-pullaway, resin smear or recession or other issues at the embedded capacitor material interfaces. A large amount of reliability testing (thermal cycle, THB, life, bend test, ESD, TMA260, solder floats, see figure 2, etc.) has been done on embedded capacitance boards internally as well as by consortium members. For the most part it has been very positive with comparable results to FR-4 material. However, this will not be discussed at this time and may be the subject of a future article.

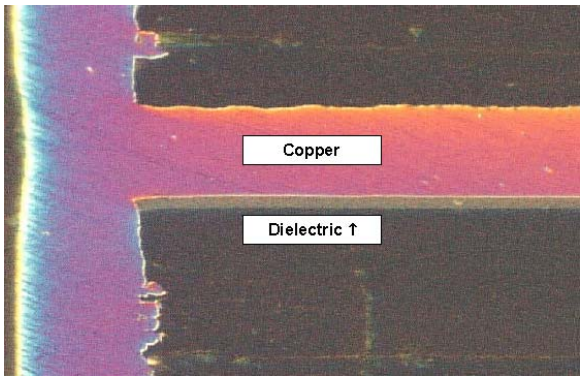

Figure 1 - Test Vehicle Cross-Sections

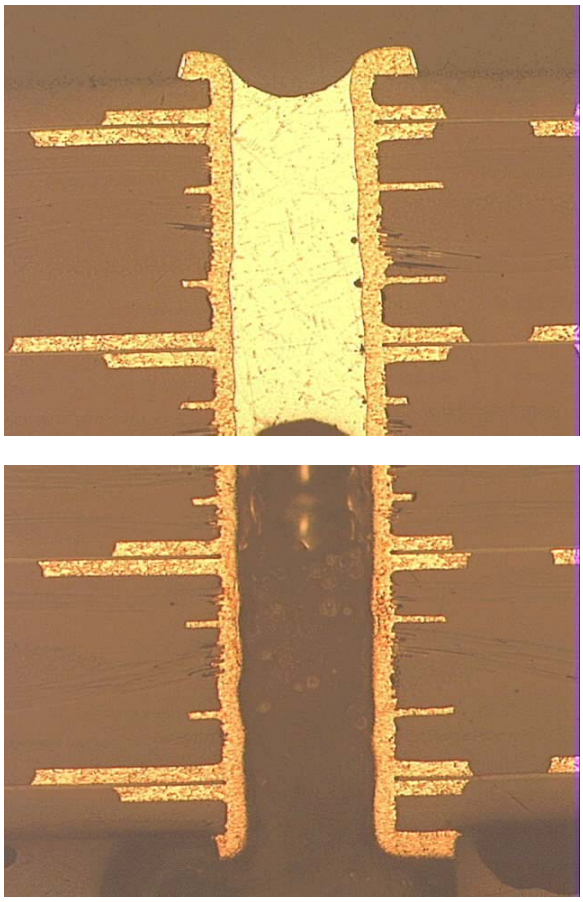

Figure 2 – Solder Float

Conclusions

1. Standard inner layer processing using thin, non-reinforced embedded capacitor material necessitates some general design guidelines which must be followed. Boards produced by this process will have exposed copper at the board edges. If a sequential lamination process is used, there are no design limitations or exposed copper at the board edges.
2. Handling of the flexible embedded capacitor material was initially a challenge for rigid board fabricators. Using leader boards and carrier panels worked well to transport the material through inner layer processing. If a sequential lamination process was used, the material handling issues were significantly reduced.
3. The fabricators' standard FR-4 process was used for all steps. For a few process steps, a slight modification was required for some or all fabricators. These included laminating resist to the board edges, non-standard phototool scaling factors, a slightly slower HiPot test speed and a reduction in HiPot test voltage.
4. Once standard design and material handling processes were defined, none of the fabricators had any significant process issues due to the embedded capacitor material.

5. Final inspection, electrical testing and cross-sections of finished product indicated that the embedded capacitor material did not create any defects or quality issues during fabrication.
6. Electrical property measurement (capacitance and dissipation factor) of the embedded capacitor laminate and finished boards showed there was no change in electrical properties or any yield loss due to board fabrication.

Summary

The embedded capacitor material was shown to be compatible with standard FR-4 processing. Sequential lamination was shown to be a good method of improving material handling and eliminating all design restrictions. The fabrication process had no effect on the embedded capacitor material electrical properties and did not create any electrical defects. As far as fabrication, embedding capacitor materials into PCBs is ready to be taken to the next level.

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