Design and Characterization of a 10 GHz Organic BGA Package

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Abstract
The design and electrical characterization of an organic BGA flip-chip package for >10 GHz operation is described. A comprehensive overview of the design process is given, including selection of substrate technology, layout strategy, electromagnetic modeling of critical signal paths, and thermal analysis. Test methods and hardware used to evaluate the frequency-domain and time-domain behaviors of the finished package are also covered. Laminate technology used for the interposer PCB was chosen for the excellent microwave properties of the dielectric material used, and its ability to realize small copper features. Layout of the interposer implements launches and transmission lines for 21 high-speed differential pairs, using structures designed to maintain a 100-ohm differential impedance environment throughout the signal path. The use of electromagnetic field solver tools (2D and 3D, quasi-static and full-wave) was essential to the design of signal launches, layer-to-layer transitions, and coupled microstrip. The BGA package houses a flip chip that dissipates about 8W of power; therefore, the design provides a low thermal resistance path from the IC to the ambient environment. A simple modification to this interposer design produced a test structure representative of the high-speed signal path(s). This test structure was characterized in the frequency domain by utilizing broadband baluns and differential microwave probes to obtain differential s-parameters. Package performance in the time domain was investigated by time-domain reflectometry (TDR) test methods, which are invaluable for locating discontinuities in the signal path.

Key words: BGA, interposer, electromagnetic simulation, flip-chip packaging, differential impedance

1. Introduction
The evolving performance requirements for the packaging of modern high-speed integrated circuits naturally accompany the advancing performance of the ICs to be packaged. Also, just as IC processes and IC design tools necessarily change over time to enable the development of new generations of ICs with higher operating speeds, so must packaging technologies and design tools progress correspondingly so that
the performance of the IC can be realized after packaging.

A project was undertaken to develop a high-performance IC package, one that would be compatible with volume solder-reflow assembly. This effort entailed advancing the capabilities of our facility in the two aforementioned areas: technology and design engineering tools. A new BGA interposer PCB technology was sought and found, and a suite of modern electrical design tools was acquired and utilized. The method and results of the initial design work that followed are now described.

2. Package Design

2.1. Substrate Technology

There are two main requirements for the BGA interposer, excluding reliability considerations. First, it must support a high density of interconnect. It must allow mating connections to the fine grid of flip-chip solder balls and preferably routing between these solder balls on their minimum pitch (250 microns). Small-diameter vias are also very desirable, especially in the “die cage” area, as they permit space-efficient local access to power and ground planes. The second sort of requirement for the interposer PCB is that it be composed of a dielectric material with low RF losses at high frequency; i.e., one with a low loss tangent at frequencies up to 10 GHz.

Several PCB vendors were evaluated and their respective capabilities compared. One vendor’s product emerged as the best match to our requirements: 3M’s VCP (Via on Chip Pitch) technology. The selected interposer PCB technology provides the desired density, achieving line widths down to 20 microns and an impressive 50-micron-diameter plated via. 

Seven layers are available for routing. Figure 1 is a photograph of a typical 7-layer board in cross-section. The dielectric material used (Microlam™) consists of an expanded PTFE matrix with added fillers; the composition achieves high reliability and good RF properties. Table 1 lists some feature sizes.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Line Width</td>
<td>20 um (minimum)</td>
</tr>
<tr>
<td>Signal Line Space</td>
<td>30 um (minimum)</td>
</tr>
<tr>
<td>Plated Via Diameter</td>
<td>50 um (nominal)</td>
</tr>
<tr>
<td>Via Pad Diameter</td>
<td>110 um (minimum)</td>
</tr>
<tr>
<td>Dielectric layer thickness</td>
<td>58 um (nominal)</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>3.3 (@ 10 GHz)</td>
</tr>
<tr>
<td>Dielectric Loss Tangent</td>
<td>.008 (@10 GHz)</td>
</tr>
</tbody>
</table>

2.2. Layout

The basic layout plans for the IC and the BGA interposer were developed concurrently. The integrated circuit to be packaged contains 21 high-speed signal pairs, various low-speed connections, and two main power supplies. Simplest, most direct high-speed connections were
accomplished by placing these around the perimeter of the flip chip; these connections were then fanned out on top layer microstrip to the edges of the BGA package. Low-speed signals, and power and ground connections were supplied to the interior of the flip chip. Many redundant power and ground connections were made over the 19 X 19 grid of BGA solder balls.

Two of the available 7 layers —- those adjacent to the central layer -- were dedicated to power planes; the central "core" layer is assigned to ground. This arrangement contributes high-quality supply bypassing to the package.

2.3. High-Speed Signal Path

Performance goals for the high-speed signal path are given in Table 2. The specified frequencies of operation and the need to design vertical transition structures in the signal path were factors that strongly influenced the decision to use electromagnetic (EM) field solver tools in the electrical design process.

Three kinds of EM field solver tools were used during the design. Table 3 compares the features of these. The 2D and 3D quasi-static field solvers were important especially in the initial stages of the structure designs. Though they are frequency-limited, they have the advantages (vs. the full-wave solver) of being somewhat simpler to use and requiring less compute time, and SPICE models can be easily produced for electrical simulation. The 3D full-wave solver was employed later in the design process to verify performance at high frequencies and to gather s-parameter data for direct comparison to network analyzer measurements taken on the finished part.

Table 3. Field solver comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>2D Quasi-Static</th>
<th>3D Quasi-Static</th>
<th>3D Full-Wave</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structure Models</td>
<td>Structures with uniform x-section</td>
<td>Arbitrary 3D</td>
<td>Arbitrary 3D</td>
</tr>
<tr>
<td>Frequency Limitation</td>
<td>Limited as with 3D, though partitioned</td>
<td>Structure dimensions must be &lt; λ/6</td>
<td>Not limited</td>
</tr>
<tr>
<td>SPICE Model Output</td>
<td>Lumped or distributed SPICE models</td>
<td>Lumped SPICE model</td>
<td>No SPICE model. Used s-parameters</td>
</tr>
<tr>
<td>Losses Modeled</td>
<td>Conductor loss over frequency. Dielectric loss @ single freq.</td>
<td>Conductor loss @ single freq. No dielectric loss.</td>
<td>Conductor and dielectric loss over frequency</td>
</tr>
</tbody>
</table>

The high-speed signal path was designed in four pieces (labeled in Fig. 2): 1) the BGA solder ball launch from the system board to the bottom of the interposer, 2) a tapered coplanar section from the top of the BGA solder balls to the bottom of the plated vias, 3) the plated vias from the bottom to the top
of the interposer, and 4) the top layer microstrip going from vias to the flip-chip IC solder ball connections. For each piece designed the goal was to provide a 100-ohm differential impedance, or as close to it as possible given constraints such as minimum via pitch and fixed BGA solder ball size. The initial design of each of these four pieces was done using the 2D field solver, treating each piece as a uniform cross-section. The BGA solder balls and the plated vias were represented as circular cross-sections of cylindrical columns. The tapered section, not being a structure with a uniform cross-section, was modeled in 2D by breaking it into a successive series of cross-sections, each designed to have a 100-ohm differential impedance. The performance of the composite taper was later checked and verified using the 3D field solvers. The fourth piece of the signal path, the embedded differential microstrip, was modeled as a group of polygonal cross-sections. Figure 3 shows the electric field associated with this differential structure as calculated by the 2D field solver.

Following the creation of the initial 2D-derived signal path pieces, the four pieces were connected together to form the complete signal path (seen in Figure 2), and then re-partitioned at points suitable for the generation of SPICE models from the quasi-static solvers. Criteria for this re-partitioning were that 1) the boundaries be located away from likely discontinuities, and 2) the length of the signal path through each 3D section should not violate the feature size/wavelength limitations of the 3D quasi-static solver. The four lumped SPICE models were connected in series and simulated in SPICE. The AC response is shown in Figure 4. Crosstalk was evaluated for adjacent signal pairs at the flip-chip IC; signal plots are shown in Figure 5.

The 3D full-wave solver was used in the final analyses to evaluate the higher frequency behavior from s-parameter data. In order to reduce compute time to reasonable lengths, the full signal path was divided along a center plane of symmetry: the differential
structure was divided by a perfect electric field wall, and simulated as a half-circuit. Figure 6 depicts this half circuit in profile. Some improvement in return loss was gained during full-wave analysis by trimming metal from the BGA ball pads and coplanar tapered section. Figure 7 shows the predicted s-parameters from full-wave analysis. The simulated performance is shown to exceed initial specification targets (Table 2).

2.4. Mechanical and Thermal

The mechanical construction of the package is straightforward, as shown in an exploded view in Figure 8. Photographs of the top (unlidded) and bottom of the package are shown in Figure 9. The Microlam™ substrate requires a bonded metallic stiffener frame as shown to provide mechanical support. The use of top layer microstrip required modification to this stiffener frame (hence its scalloped outline), which is at ground potential, in order to maintain a distance from the signal vias and lines adequate to prevent an undesired influence on the impedance of the signal path. Package specifications such...
as solder ball array size and pitch, interposer outer dimensions, and ball depopulation pattern are in accordance with JEDEC Standard 95–1 for BGA packages.

The thermal path for this flip chip package is shown in Figure 10. Note that in contrast to a typical package for a wire bonded IC, the circuitry side of the flip-chip die is face-down and the back side of the die faces the top of the package. By holding tight mechanical tolerances on the die thickness and stiffener height it is possible to achieve a low thermal resistance path from junction to case by the use of a mechanically compliant silicone rubber gasket located between the die and the package lid. This gasket must be thermally conductive but electrically insulating, since the die substrate is biased with a negative potential, and the lid is grounded.

3. Electrical Characterization

3.1. Test Structure

A test structure to enable measurements of the high-speed signal path was fabricated (Figure 11). This structure was
realized by a top-metal modification to the actual layout, and is fully representative of the simulated signal path from BGA solder ball launch to the differential microstrip.

3.2. Frequency Domain Characterization

Frequency domain characterization of the high-speed signal path on the test structure utilized a custom test set. Network analyzer measurements have traditionally been single-ended; however, the coupled nature of this signal path requires that differential s-parameter measurements be made. Since a true four-port network analyzer was not available, an approach was devised that utilized a two-port network analyzer in conjunction with broadband (to 11 GHz) baluns that perform the single-ended-to-differential conversion. Other measurement components were delay-matched, low-loss cables, differential microwave probes, and a characterization fixture PCB. Probes were positioned on the bisected line at the center of the test interposer, and outside the package on the characterization feed line. Prior to device measurements the system was calibrated to the probe tips.

S-parameter data, measured and simulated, are shown in Figure 12. Note that measurements taken were limited to 11 GHz by the bandwidth of the baluns used. Very good agreement is observed on s21/s12; response is seen to be about 1 dB down at 11 GHz. Some departure from simulated s11/s22 data is seen, though measured numbers remain good: < -20 dB to 8 GHz and < -15 dB to 11 GHz. The differences in return loss have been determined to be due to two factors: 1) the impedance of the top-layer microstrip in the interposer is about 9% high (being about 54.5 ohms, odd-mode) and some excess capacitance (about 80fF) is present at the BGA ball launch. A lumped model (Figure 13), developed after analyzing TDR data, incorporates these deviations from the simulated model. Measured and lumped model data are seen together in Figure 14; good correspondence is seen to 11 GHz.
3.3. Time Domain Characterization

Time domain reflectometry measurement techniques are useful for quantifying and physically locating impedance discontinuities in a high-frequency interconnect structure. Additionally, differential TDR measurements can be readily performed using available time domain instrumentation. In this case, a Tektronix 11800 oscilloscope with high-speed sampling heads was used, with essentially the same fixture, cabling and differential microwave probes as used for the frequency domain test set. The TDR measurements taken enabled the determination of the lumped model of Figure 13 by revealing the as-fabricated characteristic impedance value of the package microstrip and indicating the location of the excess capacitance at the BGA ball launch. TDR data is shown in Figure 15; the measured TDR data is shown against the signature of the lumped model, and very good correlation is observed.

4. Conclusion

The initial use of an advanced PCB technology and a suite of modern EM structure simulator tools led to a first-time success in the design and development of a new BGA package with >10 GHz performance. In addition to the characterization data taken on the test structure, the actual integrated circuit packaged with this new interposer design has demonstrated performance over 12.5 GHz on the bench.

Furthermore, characterization of the prototyped design has “closed the loop,” indicating areas of the package to be targeted for improvement on next, higher frequency designs.

5. Acknowledgements

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6. References
